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INTEGRATED INJECTION LOGIC TECHNOLOGY DEVELOPMENT

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This report describes the progress in a program to determine the characteristics and limitations of the bipolar integrated injection logic technology as applied to the problem of implementing low power, large scale random logic arrays with low fabrication costs. The activity has concentrated in four areas of integrated injection logic study and development. First, a device and circuit modeling task was undertaken to derive analytical expressions for integrated injection logic design parameters including transistor current gain, fanout, minimum → CONT

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propagation delay, and delay-power product. The calculated properties of integrated injection logic logic gates fabricated on epitaxial wafers as well as uniformly doped nonepitaxial wafers are summarized. Second, the integrated injection logic fabrication process was re-evaluated on optimizing the current gain of npn and pnp transistors. The experimental approach was concentrated on the use of a two-step boron diffusion process for increasing the pnp injection efficiency at no loss in npn current gain. Third, a test chip incorporating the two-step boron diffusion process was designed to obtain experimental measurement of integrated injection logic logic gates used to implement typical random logic functions, such as binary counters and serial shift registers. Fourth, a set of preliminary test results was summarized for devices fabricated with the same set of photomasks on epitaxial as well as nonepitaxial wafers. The results indicate that for the epitaxial devices, minimum gate delays of 15 ns and delay-power products of 0.35 pJ are representative. For the nonepitaxial devices, the corresponding values are 25 ns and 0. pJ, indicating that the performance of the simpler process may approach that of the former.

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SECTION 1

INTRODUCTION AND SUMMARY OF PROGRESS

This report describes the technical progress on Contract DAAB07-75-C-1361, entitled "Integrated Injection Logic Technology Development." The objectives of this contract include the following:

(1) To perform an analysis of the tradeoffs involved in the design of I^2L logic for the purposes of achieving

- the minimum power consumption
- the minimum delay time
- the maximum logic gate packing density consistant with yield

(2) To design, fabricate and evaluate I^2L test chips to establish device performance parameters and scaling laws for LSI design.

During the first half of the contract, the technical effort has been directed toward both analysis of the tradeoffs indicated above, as well as preliminary experimental work to establish the wafer process parameters and the I^2L logic performance parameters of interest prior to the design activity. The progress made to date can be grouped into three categories and is summarized in the following discussion.

1.1 I^2L TEST CHIP DESIGN

An analysis was made of the basic I^2L logic gate in which the dependence of the npn and pnp terminal currents on a variety of process parameters was evaluated. This study included the variation of npn and pnp current gains with typical variations in wafer process parameters, such as impurity profiles, material parameters, and layout geometries. In addition, the minimum delay per gate and the delay-power product are described analytically in terms of npn and pnp device parameters. It is shown that the realization of high

current-gain transistors is desirable to optimize these performance parameters, consistent with the limitations of the wafer fabrication process. A portion of this analysis included an evaluation of the uniformly doped nonepitaxial substrate fabrication approach. For this case, the lifetime of holes in the substrate τ_p was identified as a critical variable and design curves were generated with τ_p as a parameter. Also, the value of maximum npn basewidth was determined to be approximately 0.6 μm for nonepitaxial process in order to achieve a minimum β, which is well within reasonable process control.

1.2 I^2L WAFER PROCESS DESIGN

The wafer process used for fabrication of the test chips, on both epitaxial and nonepitaxial substrates, was studied. Based on the results of the analysis and modeling effort, several process options were identified to increase I^2L gate performance, primarily by increasing transistor current gain.

The major process options include a double diffused npn base for optimal npn β and pnp α, the use of an ion-implanted base to improve npn gain uniformity, and the option to integrate Schottky barrier diodes at the npn collectors. All of the above mentioned options can be accomplished by a simple sub-set of the normal I^2L photomask sequence.

1.3 I^2L TEST CHIP DESIGN

The design test chip to be delivered to ECOM is described. The test chips contain circuitry for the purpose of characterizing delay-power product and minimum delay time, as well as functional circuitry. Functional circuitry include four 3-bit binary counters and two 32-bit serial shift registers. Designs representative of both 5 μm and 7.5 μm design rules are included on this chip to determine performance versus yield tradeoffs. The test chip fabrication is underway, and test data will be available during the second half of the contract.

1.4 PRELIMINARY EXPERIMENTAL RESULTS

Experimental results have been limited to previously designed test chips. This activity has concentrated on a comparison of the performance parameters of the epitaxial process and a noneptitaxial process fabricated on 0.1 to 0.3 ohm-cm bulk silicon. The preliminary test results indicate that the current gain of nonepitaxial devices is about 1/2 to 2/3 the value of identical geometry devices fabricated on epitaxial substrates. A corresponding reduction in the switching performance parameters of the nonepitaxial ring oscillators was seen. Delay-power products of 0.5 pJ and minimum delay times of 25 ns were seen to be representative of the first lot of nonepitaxial devices. For ring oscillators of the identical design fabricated on epitaxial wafers, delay-power products of 0.35 pJ and minimum delay times of 15 ns were typical.

SECTION 2

I^2L DEVICE DESIGN

2.1 DEVICE MODELING

2.1.1 PNP Transistor

The I^2L cell consists of an npn transistor and a lateral pnp current source. The pnp collector and the npn base coincide and are formed by the same p-diffusion. Figure 2-1 shows the cell geometry and the current components in the transistors. The dc characteristics of the pnp transistor will be described here and the remainder of the chapter will be used for the npn analysis.

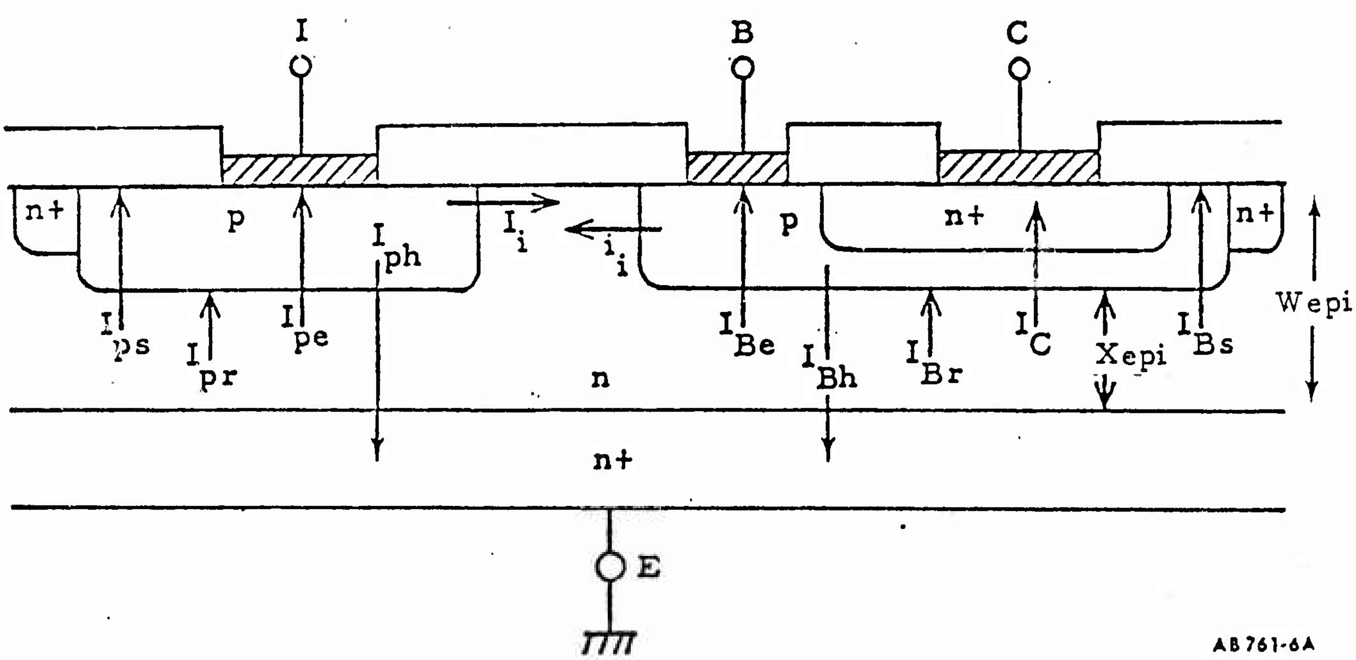

Figure 2-1. A schematic of the I^2L unit logic cell, showing the injector and the npn base and collector terminals. The arrows indicate the direction of carrier injection.

The lateral pnp has been discussed by Chou in considerable detail.[1] Therefore, only a brief description will be given here. The current components include:

I_{ph} : hole injection into the epi and substrate

I_{pe} : electron injection into the diffused p-region

I_{pr} : recombination in the pn junction depletion layer

The hole injection current I_{ph} supplies recombination current (loss) in the n+-substrate, at the n-n+ interface, and the n-epi region. This current component has been derived by Dutton and Whittier.[2] The current $I_{p,e}$ is due to recombination at the contact and the oxide-silicon interface. For a typical clean oxide with a surface recombination velocity of ~300 cm/s or lower, it can be shown that recombination at the oxide-silicon interface can be neglected. The above current components may be written as,

$$I_{ph} = I_{BO1}\, e^{qV_{EB}/kT} \tag{2-1a}$$

$$I_{pe} = I_{BO2}\, e^{qV_{EB}/kT} \tag{2-1b}$$

$$I_{pr} = I_{BO3}\, e^{qV_{EB}/2kT} \tag{2-1c}$$

where V_{EB} is the pnp emitter-base voltage. Using the results of References 1 and 2, the following data are calculated for an injector area of $17.5 \times 10\ \mu m^2$:

$$I_{BO1} = 6 \times 10^{-18}\ A$$

$$I_{BO2} = 1.7 \times 10^{-18}\ A$$

$$I_{BO3} = 7.3 \times 10^{-13}\ A.$$

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1. Sunlin Chou, Solid-State Electron. 14, 811 (1971).
2. R. W. Dutton and R. J. Whittier, IEEE Trans. Elec. Devices, ED-16, 458 (1969).

The design parameters used in the above calculations are: epi concentration, $N_{epi} = 2.2 \times 10^{16}/cm^3$; p-diffusion depth, $X_B = 1.8 \mu m$; boron surface concentration $= 2 \times 10^{18}/cm^3$; $W_{epi} \sim 3\ \mu m$ (see Figure 2-1); and a contact area of $5 \times 10^{-7} cm^2$. The npn base profile is assumed to be a Gaussian distribution, and a diffusion length ($Dt = 1.96 \times 10^{-9} cm^2$) was used, corresponding to a 1.4-hour drive-in at 1100°C. Note that the contact recombination current is about 30% of the hole current and can be reduced by minimizing the contact area.

The lateral pnp collector current has been calculated by Chou and may be written as

$$I_{CP} \approx I_{PO} \exp (q V_{EB}/kT) \tag{2-2}$$

The parameter I_{PO} is a strong function of the pnp base width, W_{BP}, and the epi concentration, N_{epi}. For $N_{epi} \sim 2 \times 10^{16}/cm^3$, we calculate a value of $I_{PO} \sim 2 \times 10^{-17}$ A.

An important parameter that to a large extent determines power consumption per cell is the pnp common-base forward current gain, α_F.

$$\alpha_F = \frac{I_{CP}}{I_{CP} + I_{BP}}$$

A computer program was used to calculate the pnp (as well as the npn) current components and current gain. Figures 2-2 and 2-3 show the variation of α_F with the diffusion depth X_B and with the epi concentration, N_{epi}. The lateral p-p spacing, W_O, was assumed 5 µm and 7 µm.

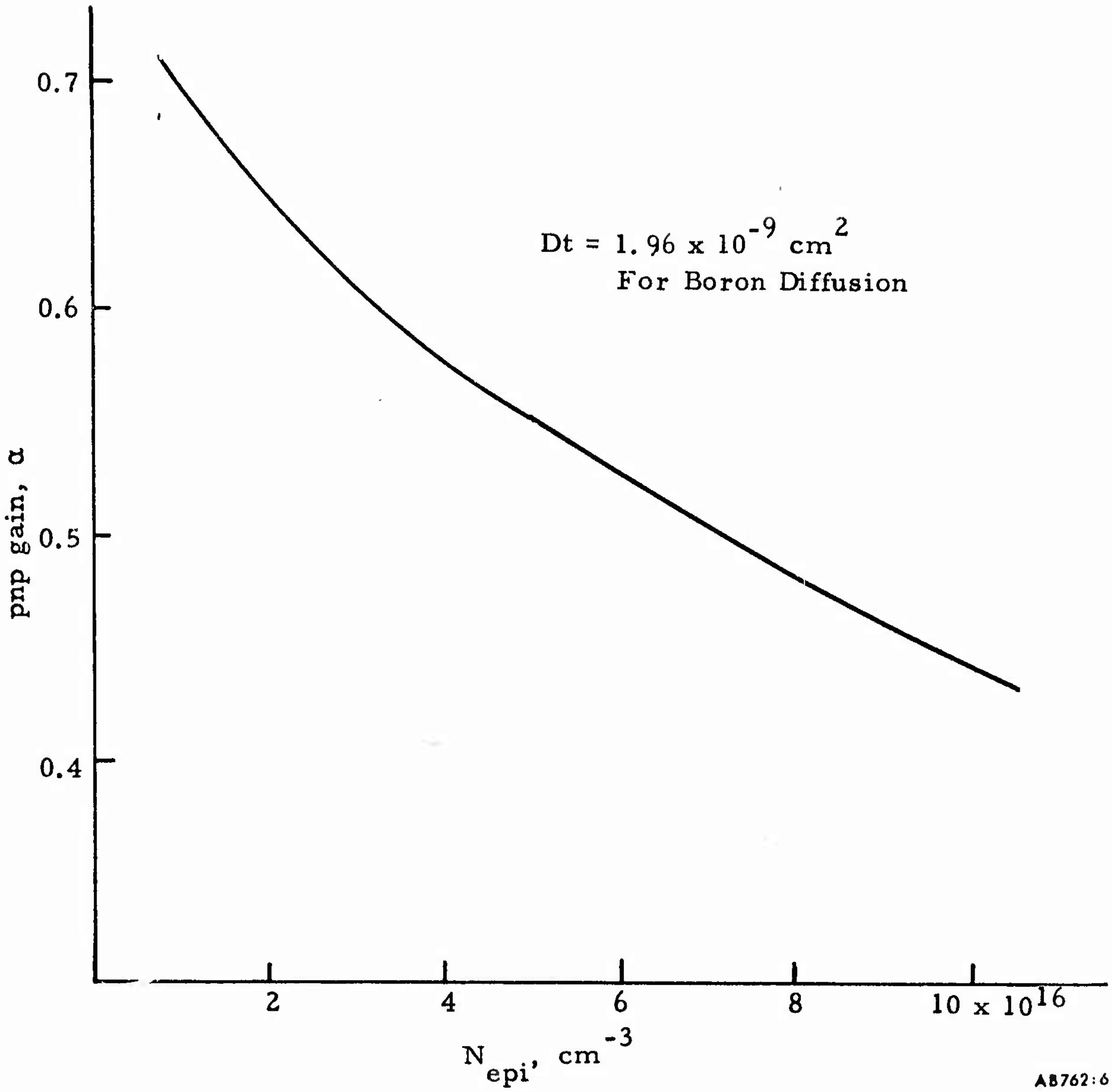

Figure 2-2. Variation of pnp current gain α with epi concentration, N_{epi}. The drop in α is mainly due to the decrease in base diffusion depth as N_{epi} increases. The p-diffusion time and surface concentration are kept fixed.

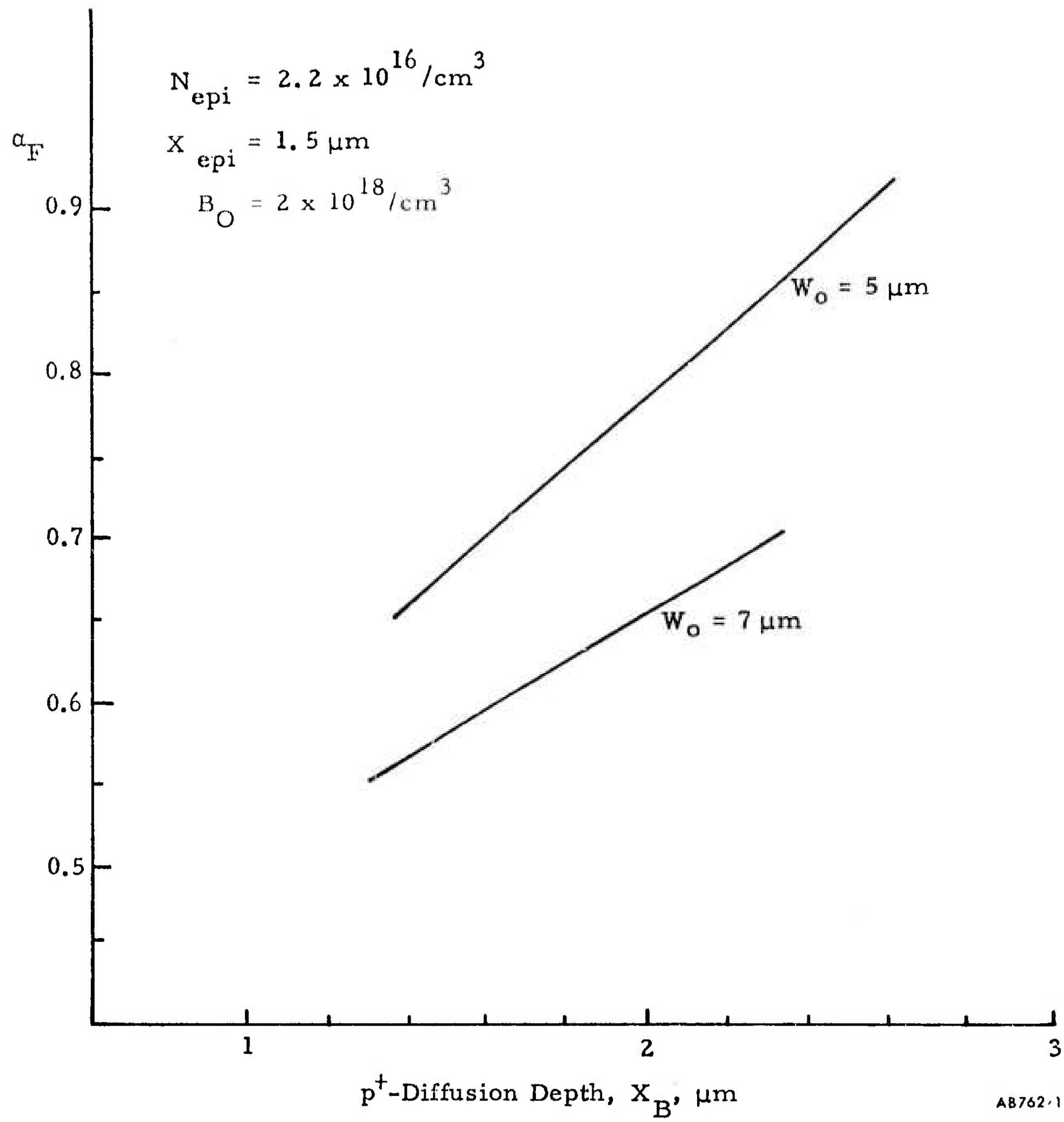

Figure 2-3. Variation of the pnp forward current gain with p-diffusion depth.

Finally, high-level injection effects become important when the injected hole concentration is comparable to the emitter majority carrier concentration. That is, high-level injection occurs when $p_n = N_{epi}$, where:

$$p_n = \frac{n_i^2}{N_{epi}} \exp(qV_{EB}/kT)$$

Hence, the voltage which separates low-level from high-level injections is approximately

$$V_{HL} = \frac{2kT}{q} \ln (N_{epi}/n_i) \qquad (2\text{-}4)$$

The room-temperature value of V_{HL} is computed below:

N_{epi}, cm^{-3}	V_{HL}, Volts
1.5×10^{15}	0.60
1.5×10^{16}	0.72
1.5×10^{17}	0.84

For $V_{EB} \geqslant V_{HL}$, the pnp collector current Eq. (2-2) should be multiplied by a correction factor F_C (V_{EB}) which is given by Chou. For $V_{EB} >> V_{HL}$, I_{CP} varies as $\exp(qV_{EB}/2kT)$ due to high-level injection effects.

2.1.2 NPN Transistor.

The I^2L cell contains an inverse-operated npn (collector up) and consequently offers a low current gain-bandwidth product as compared to other standard bipolar technologies. A low gain would mean a higher-than-desired power consumption, whereas a low bandwidth would result in long switching times. An extensive analysis of the I^2L basic cell performance characteristics was undertaken in order to determine the process parameters that can be best

utilized to optimize the switching speed and power consumption of the I^2L gate. A brief description of the results is given below.

Figure 2-1 shows the npn transistor and relevant current components. The collector current is given by

$$I_C = I_{CO} \exp (qV_B/kT) \tag{2-5}$$

where

$$I_{CO} = \frac{qn_i^2 S_C D_e}{\int_0^W N_B(x)\,dx}$$

and S_C is the collector area, D_e is the electron diffusion constant, $N_B(x)$ is the base net doping concentration per unit volume, W is the base width, n_i is the intrinsic carrier concentration, and V_B is the base-emitter voltage.

The base current components are similar to those calculated for the pnp transistor:

$I_{Be} = (I_{BCO} + I_{BSO}) \exp(qV_B/kT)$		electron injection	(2-6a)
$I_{Bh} = I_{BhO} \exp (qV_B/kT)$		hole injection	(2-6b)
$I_{Br} = I_{SCO} \exp(qV_B/2kT)$		space-charge recombination	(2-6c)

where I_{BCO} refers to recombination at the base contact and I_{BSO} refers to oxide-silicon interface recombination. Typical computed values for our n+ diffused collar, single collector, minimum geometry device are:

$I_{BCO} = 1.7 \times 10^{-18}$ A $\qquad I_{BhO} = 2.8 \times 10^{-17}$ A

$I_{BSO} = 2 \times 10^{-19}$ A $\qquad I_{CO} = 3 \times 10^{-16}$ A

$I_{SCO} = 3 \times 10^{-12}$ A

The parameter I_{CO} is the exponential term multiplier in Eq. (2-5).

The npn current gain is given by

$$\beta = I_C/I_B$$

The hole current I_{Bh} constitutes most of the base current at voltages $V_B > 0.6\,V$, which corresponds to a collector current of approximately $2\,\mu A$. Hence, a very effective method of increasing β is to reduce I_{Bh}. Also, I_C may be increased by reducing the integral $\int_0^W N_B(x)\,dx$ over the base. Therefore, process parameters having a substantial effect on the npn gain are: the base and collector profiles, the epi doping, N_{epi}, and the epi thickness below the base p-diffusion, X_{epi}. An NRTC computer program was used to evaluate the effect of the above parameters on the npn gain. Some of the results are given in Figure 2-4 and Figure 2-5.

Using actual process parameters for the epitaxial layer and for the base and collector diffusions, the dc characteristics of the npn transistor for an I^2L test cell were calculated. The computer results agree very well with the measured experimental dc characteristics of the I^2L test cell, as discussed in Section 5.

2.1.3 I^2L Logic Gate Transient Response

The transient response of the I^2L gate determines the delay per gate in digital circuit applications. The npn will switch from off (i.e., nearly zero base voltage) to fully on (i.e., a base voltage of $\leq 1V$). At low current levels, charge must be supplied to charge up the npn capacitance to its operating voltage. At high operating currents, where the capacitive charging time is small, electrons and holes must be stored in the npn emitter-base regions before steady-state terminal currents can flow. In this case, the delay per gate is fundamentally the minimum achievable delay for a given design. For I^2L to exceed the performance available from competing technologies, the delay and power consumption per gate should be minimized for both low and high current applications. The reduction of the minimum propagation delay time is considered subsequently.

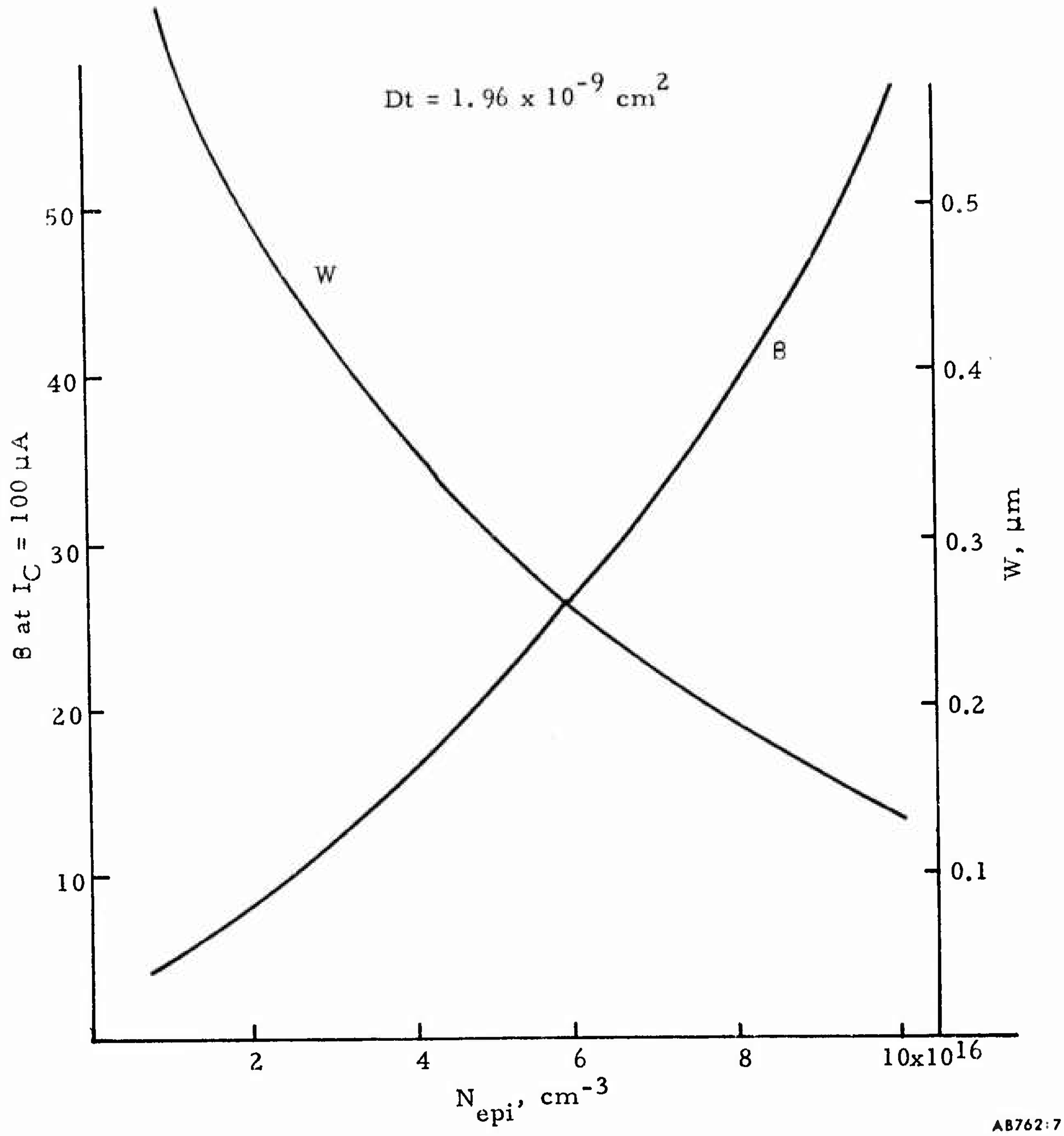

Figure 2-4. Variation of the npn base-width, W, and current gain, β, as a function of the epi doping concentration, N_{epi}. The diffusion times and temperatures for the collector and base diffusions are kept constant.

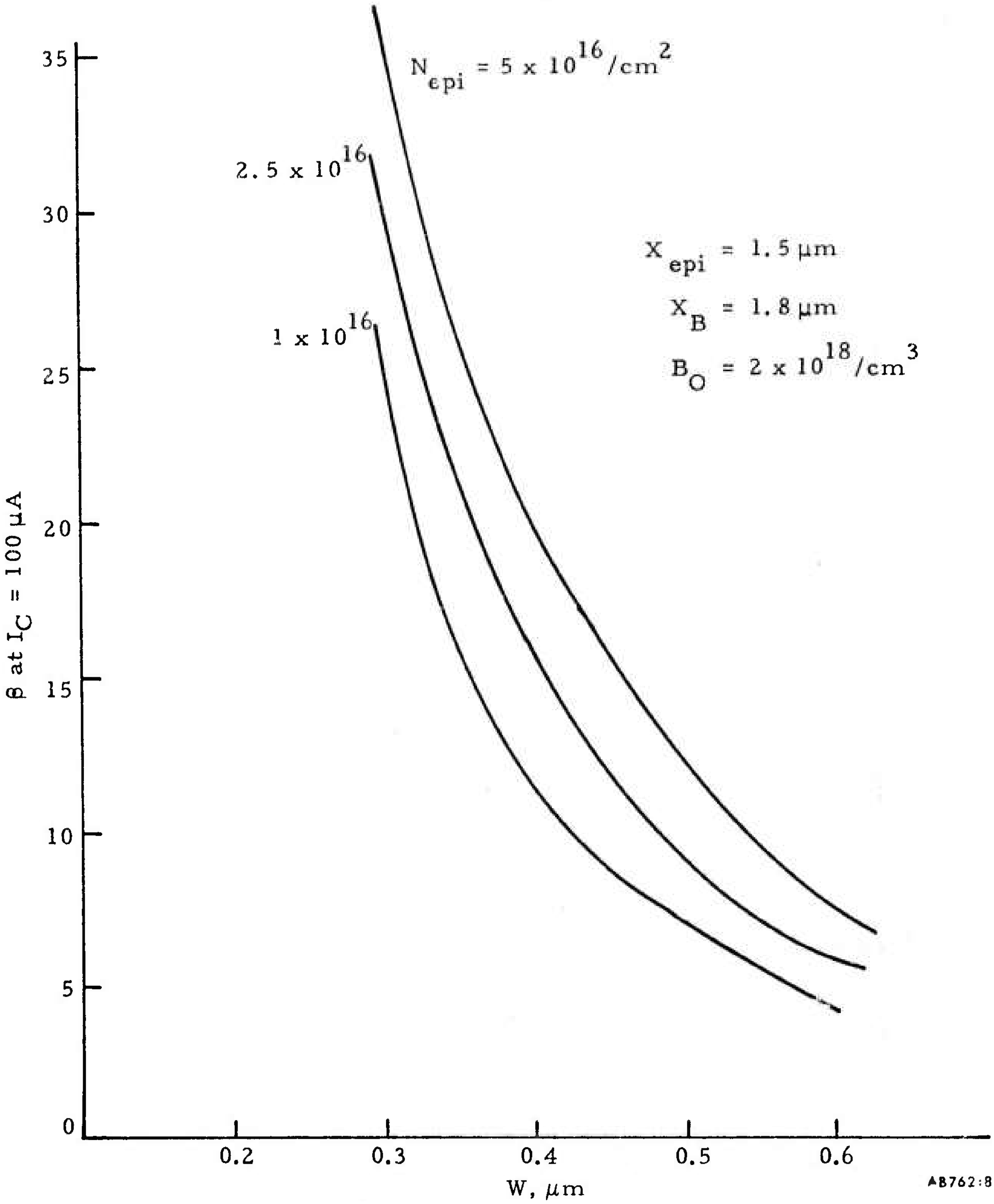

Figure 2-5(a). Variation of the npn current gain, β, with the base-width, W, keeping the boron junction depth X_B, surface concentration B_O, and X_{epi} fixed.

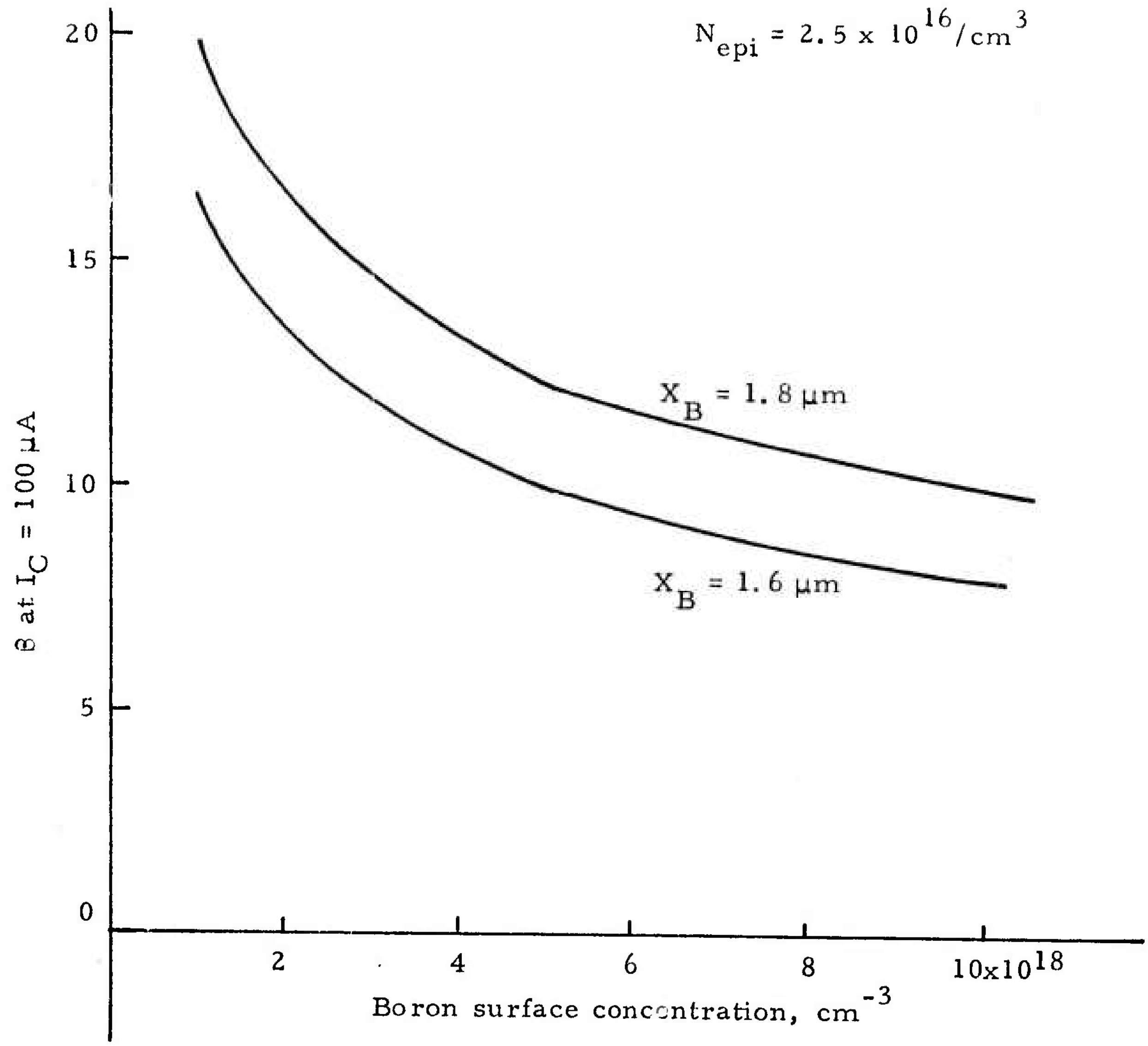

Figure 2-5(b). Variation of npn gain with the boron surface concentration, B_O, keeping X_B and N_{epi} fixed. The epi thickness, X_{epi}, underneath the p-diffusion is 1.5 μm for both curves.

The dynamic behavior of the I^2L gate was calculated from the charge control model of the npn transistor. Both the small-signal frequency response and the switching transient response of the npn transistor were analyzed. The minimum delay per stage was calculated by considering the transient response of three cells in an inverter chain.

Figure 2-6 shows three cells in an inverter chain. Assume initially transistors T1 and T3 are on and T2 is off. At $t = 0$, T1 is suddenly discharged, causing T2 to turn on. As T2 becomes saturated, T3 turns off at time t_d, where t_d is one delay-time per stage. In this configuration, the injectors supply the base as well as the collector currents of the npn transistors. (The term injector current here refers to the collector current of the pnp.) We will assume that charge storage in the npn transistor can be described by a single storage time, τ_s. For standard I^2L, $\tau_s = \tau_E$, where τ_E is the emitter storage time.

Referring to I^2L cell T2, as the npn base voltage increases, the pnp approaches saturation and some back-injection occurs from the pnp collector into the base. Denoting this back-injection by i_i, the steady-state terminal relation is

$$I_i - i_i = I_B \qquad (2-7)$$

where $I_B = I_{BO} \exp(q V_B / kT)$.

For a given injector voltage (i.e., I_i), Eq. (2-7) and the npn emitter-base geometry and pnp base-width determine the base current and base charge. During the turn-on transient, the injector current is given by:

$$I_i = i_i(T2) + I_B(T2) + \frac{d q_B(T2)}{dt} \qquad (2-8)$$

$$I_B(T2) = \frac{q_B(T2)}{\tau_s}$$

with the initial conditions that at $t = 0$

$$I_B(0) = 0$$

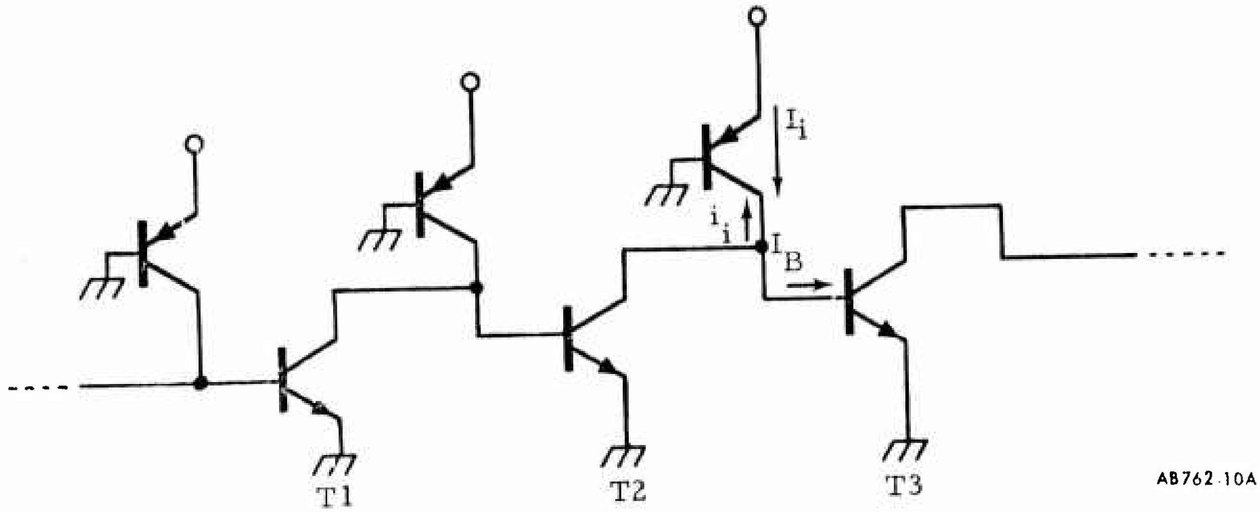

Figure 2-6. An I^2L inverter chain.

The transistor T3 will start turning off as $I_C(T2)$ increases, where $I_C(T2)$ is the time-dependent collector current of T2. During turn-off of T3, the injector supplies current both to T2 and T3. Hence

$$I_i = \frac{dq_{B3}}{dt} + \frac{q_{B3}}{\tau_s'} + I_C(T2) \tag{2-9}$$

with the initial condition that at $t = 0$, $I_B(T3)$ is given by Eq.(2-7). The time t_d when T3 is turned off is obtained from the solution of Eqs. (2-8) and (2-9).

Figure 2-7 shows the calculated delay-time, t_d/τ_s', plotted as a function of the effective current gain $\bar{\beta}$, where

$$\bar{\beta} = \frac{\beta}{1 + I_{PO}/I_{BO}} = \frac{I_{CO}}{I_{BO} + I_{PO}} \tag{2-10}$$

$$\tau_s' = \frac{\tau_s}{1 + I_{PO}/I_{BO}} = \tau_s \bar{\beta}/\beta \tag{2-11}$$

Clearly, as $\bar{\beta}/\beta$ increases, τ_s' increases and the delay-time t_d increases. For a given injector with the smallest possible geometry, $\bar{\beta}/\beta$ increases as I_{BO} increases. The latter occurs as the base area increases. For minimum delay, therefore, it is necessary to keep the base area small by making the minimum geometries and the fan-out as small as possible.

Let us now consider the effect of increasing the current gain, β, on the delay time. First, if I_{BO} is kept fixed and β is increased by narrowing the base width, τ_s' remains unchanged but t_d will decrease due to the increase in $\bar{\beta}$. If $\bar{\beta} \leq 2$, the increase in β will have a significant effect on t_d. For $\bar{\beta} > 6$, t_d is not appreciably affected by the increase in β. However, if β is increased by decreasing I_{BO}, both τ_s' and ratio t_d/τ_s' will decrease, resulting in a very significant change in the minimum delay time. The decrease in I_{BO} can be achieved by reducing the epitaxial layer thickness.

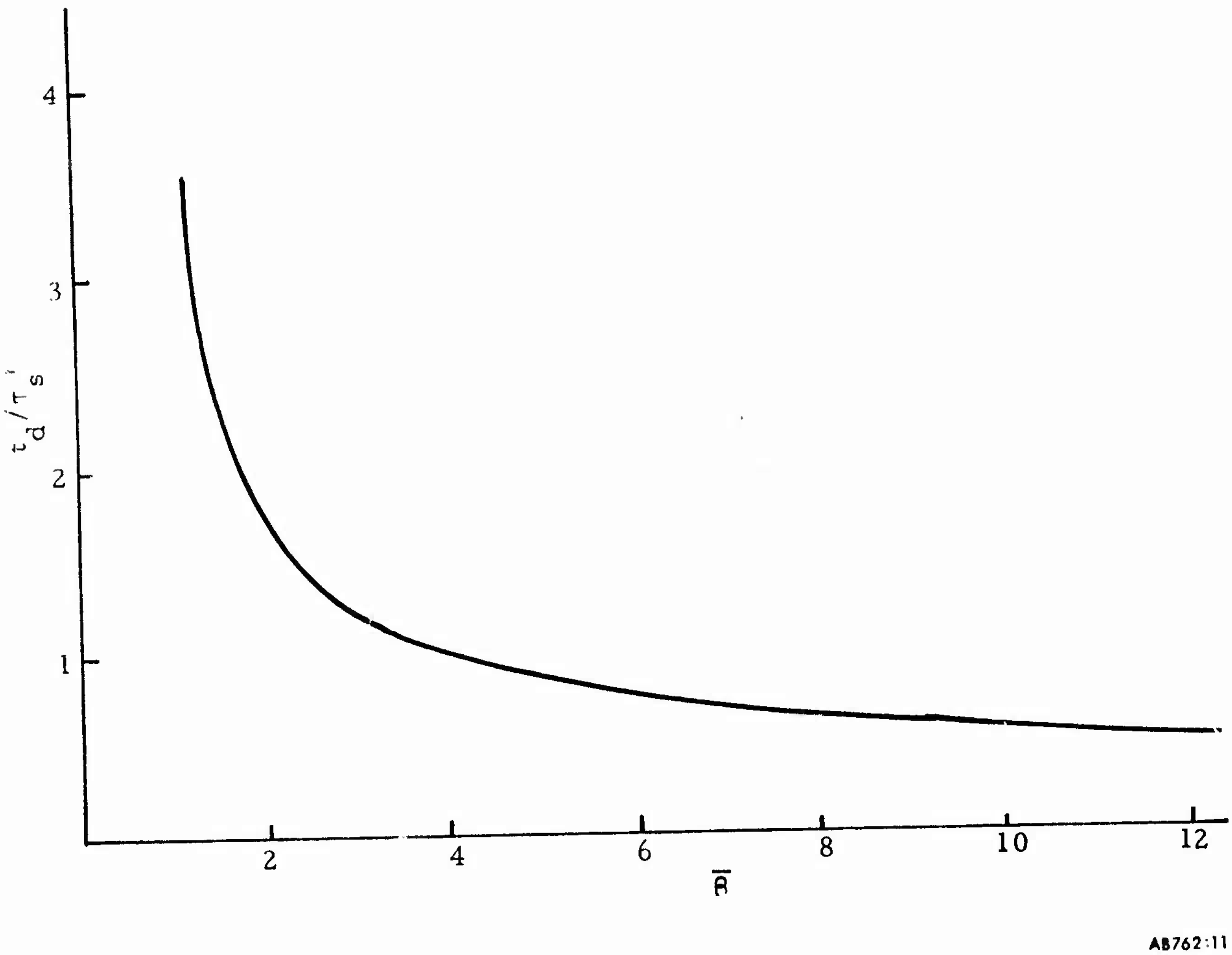

Figure 2-7. Variation of the effective delay, t_d/τ_s', with the composite gain $\overline{R}$

2.2 DEVICE PARAMETER OPTIMIZATION

The dynamic behavior of the I^2L gate and its power consumption are affected by both the pnp and npn transistor design. Both high-gain pnp and npn transistors are needed if the power consumption is to be reduced. The parameter I_{PO} to a large extent determines the pnp current gain, and as discussed in the last section, the ratio I_{PO}/I_{BO} and the npn effective gain $\overline{\beta}$ have to be large in order to reduce the minimum delay per gate. On the other hand, a low delay-power product can be achieved by a small npn emitter-base junction capacitance. At very low current levels, the npn turn-on delay is primarily due to the time needed to charge the emitter-base junction capacitance to the steady-state base voltage given by Eq.(2-7). The reduction of the capacitance, in general, will result in some sacrifice in the npn gain, β. Therefore, the design optimization steps will depend on the particular application and operating currents. Since the pnp supplies the emitter-base capacitance charge, a high-gain pnp should have very favorable effects on the speed-power product as well as the minimum delay.

2.2.1 Design Optimization for Minimum Delay.

From the results of Section 2.1.2, the minimum delay per stage t_d is reduced by increasing I_{PO} and β and/or reducing τ_E. I_{PO} is increased by reducing the pnp, p-p spacing and the epi concentration and by increasing the p-junction depth. β is increased by making the npn base width narrower and by reducing I_B. The reduction of τ_E will result in higher I_B, lower β, and higher power consumption, and is therefore not desirable.

An effective method of reducing the delay time is to incorporate an n+-buried layer. This will suppress hole injection into the epi layer (emitter). The advantages of this process include (1) the npn β is increased; (2) power dissipation in the npn emitter and pnp base is reduced; (3) a buried layer should have a lower τ_E, and because of a higher β, a reduced t_d should result; and (4) if the buried layer is sufficiently effective to make $I_{Bh} < I_{Be}$, then the base storage

time will be essentially limited by charge storage in the extrinsic base. The latter storage time is $W_B^2/2D_e \sim 4$ ns, as compared to $\tau_E \sim 50$-100 ns. The drawback is an increase in the depletion region capacitance because of the higher impurity concentration. However, for operation at the higher currents (100-500 μA) to achieve minimum delay, the diffusion capacitance term dominates the npn input capacitance.

2.2.2 Delay-Power Product

To optimize the design for a low delay-power product, the npn emitter-base capacitance should be reduced. For I^2L with n+ collars, the primary contribution to capacitance is from the collar side walls where both boron and phosphorus concentrations are high. In addition, at low currents the side walls contribute a substantial space-charge recombination current. By using oxide isolation in place of n+ diffused isolation, both problems can be eliminated.

When the npn base voltage is high, the injector supplies current for charge storage in the npn as well as pnp base and emitter regions. On the other hand, when the pnp provides the collector current of a saturated npn, most of the power is spent in supplying recombination in the pnp. Assuming each npn is operated at a 50% duty cycle, it can be shown that the power dissipation is given by

$$P = \frac{1}{2} I_i V_i \left(1 + \frac{2S_I}{S_E} \frac{I_{BO}}{I_{PO}} + \frac{I_{BO}}{I_{BO} + I_{PO}}\right) \tag{2-12}$$

where I_i is the injector current (pnp collector current), S_I and S_E are the pnp and npn emitter areas, and V_i is the injector voltage.

To a first-order approximation, the time required to charge the npn emitter-base capacitance, C, to voltage V_B is

$$t = C V_B / I_i \tag{2-13}$$

Hence, the delay-power product is given by

$$P \cdot t_d = \frac{1}{2} C V_i V_B \left(1 + \frac{2S_I}{S_E} \frac{I_{BO}}{I_{PO}} + \frac{I_{BO}}{I_{BO} + I_{PO}} \right) \tag{2-14}$$

where V_B is given in terms of V_i by the relation (see Eq. 2-7),

$$I_{PO} \exp(q V_i/kT) = (I_{PO} + I_{BO}) \exp(q V_B/kT) \tag{2-15}$$

Since $V_i \approx V_B$, the term $1/2\, C V_i V_B$ is approximately the energy stored in the npn emitter-base capacitance. Eq. (2-14) indicates that for $I_{PO} >> I_{BO}$, the minimum delay-power product is equal to the energy stored in the npn emitter-base capacitance. Figure 2-8 shows a plot of normalized power-delay product as a function of I_{PO}/I_{BO}. Note that for $I_{PO} > 1.6\, I_{BO}$, the reduction in delay-power product is not too dramatic as I_{BO} decreases. However, if I_{BO} is reduced by using a buried-layer approach, the npn input capacitance C, due to the junction depletion capacitance, increases as $\sqrt{N_{epi}}$. Therefore, if a buried-layer approach is used for a low delay-power product design, care must be taken to ensure the buried-layer and base diffusions do not intersect at a doping greater than about 5×10^{16} cm^{-3}.

For low delay-power product, then, the following design rules may be used:

High-gain pnp:

- p-diffusion: $X_B = 1.8\ \mu m$, 2×10^{18} cm^{-3} surface concentration
- $N_{epi} = 1 \times 10^{15} - 1 \times 10^{16}$ cm^{-3}
- p-p spacing: 5 µm

High-gain npn:

- Controlled n+-buried layer emitter
- Oxide isolation (Optional)
- 0.4 µm basewidth (This basewidth contributes to high gain without excessive process control.)

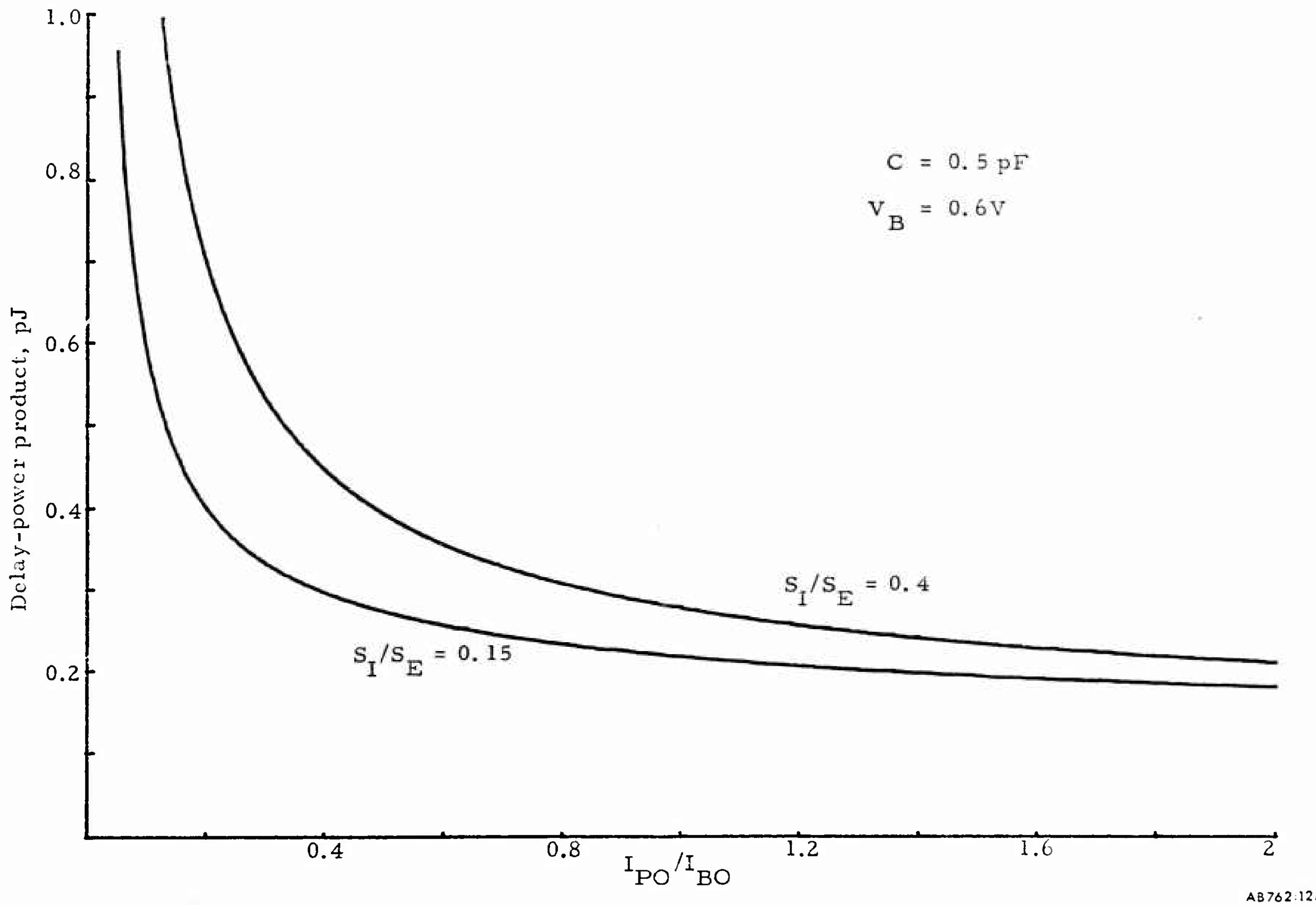

Figure 2-8. Variation of delay-power product with I_{PO}/I_{BO}, normalized to C = 0.5 pF and V_B = 0.6V. For other values of C and V_B, multiply by $(C/0.5)(V_B/0.6)^2$.

2.3 I^2L DESIGN FOR BULK (NONEPITAXIAL) MATERIAL

In the previous sections the analysis and design of I^2L cells on epitaxial silicon was considered. For low-speed applications where fabrication cost is an important factor, I^2L circuits built on bulk single crystal silicon substrates could offer cost savings, higher yield, and faster turn-around. Some features of the bulk design are briefly discussed below.

Most of the results developed in the previous sections are directly applicable to a bulk design process as well. The expressions for the pnp and npn collector current are still valid, with N_{epi} replaced by the bulk substrate doping, N_S. The design curves for minimum delay and power-delay product can be directly used once the ratio I_{PO}/I_{BO} and β are calculated for the bulk design.

The hole current injected into the npn emitter is given by

$$I_{Bh} = I_{BhO} \exp(qV_E/kT)$$

$$I_{BhO} = \frac{n_i^2}{N_S}\sqrt{\frac{D_p}{\tau_p}}\; S_E$$

To increase gain, I_{BhO} should be reduced, which can be achieved by increasing τ_p and N_S. The increase in N_S will also lower the pnp collector current and therefore will not affect the ratio I_{PO}/I_{BO}. That is, increasing the substrate doping will result in higher npn gain, but will not reduce speed-power product. In fact, the capacitance of the npn emitter-base junction goes up as N_S increases, thus resulting in a higher power-delay product. One faces a situation where a compromise must be made between a high npn gain and a low power-delay product.

On the other hand, if τ_p increases, β_{npn} and α_{pnp} will increase, but the pnp collector current will not be affected. Consequently, the ratio I_{PO}/I_{BO} will increase, thus resulting in lower delay-power product. Hence a long life-time material is desirable both for high gain and low delay-power product.

The design rules for low power-delay product for bulk I^2L now become fairly simple and straightforward:

(1) Choose a high quality material with long minority-carrier lifetime. The donor concentration is chosen to make the maximum circuit fanout feasible. (If β is the gain for a single collector npn, then β should be designed for $\beta/N \geqslant 2$, where N is the fanout.)

(2) Use 1.8 μm boron diffusion depth for higher pnp gain and larger (I_{PO}/I_{BO}) ratio.

(3) A narrow base is desired for high npn gain. If the basewidth can be controlled accurately, the substrate doping may be reduced to achieve a lower emitter-base capacitance. An ion-implanted npn base is desirable to increase collector current and to reduce the effect of npn gain fall-off at low currents due to the space charge components of npn base current.

(4) Use oxide isolation to reduce depletion layer capacitance and to limit space charge recombination components of npn base current.

Figures 2-9 to 2-14 show some of the computed pnp and npn characteristics for minimum-dimension I^2L cells. The variations of the npn and pnp collector currents and β and α with process parameters such as substrate doping, boron surface concentration, etc., are given in the figures.

Of special interest is the requirement on npn basewidth to achieve a minimum current gain (i.e., $\beta \approx 2$). For a process using a fixed base drive-in ($Dt = 1.96 \times 10^{-9} cm^2$), Figure 2-9 indicates that the use of a wafer with bulk doping between 10^{16} and $3 \times 10^{16} cm^{-3}$ results in an npn basewidth of 0.6 μm to 0.4 μm and a corresponding β of 2.5 to 8 at 100 μA. Figure 2-12 indicates the dependence of npn gain on basewidth for a base surface concentration of $2 \times 10^{18} cm^{-3}$ and a bulk doping of $10^{16} cm^{-3}$, at two values of collector current, 1 μA and 100 μA. For the worst case at 1 μA, a maximum basewidth of approximately 0.6 μm is allowable to achieve a minimum npn gain. Hence, a nominal control of npn basewidth of 0.4 μm to 0.6 μm is adequate to achieve current gains of 2-4 at a collector current of 1 μA.

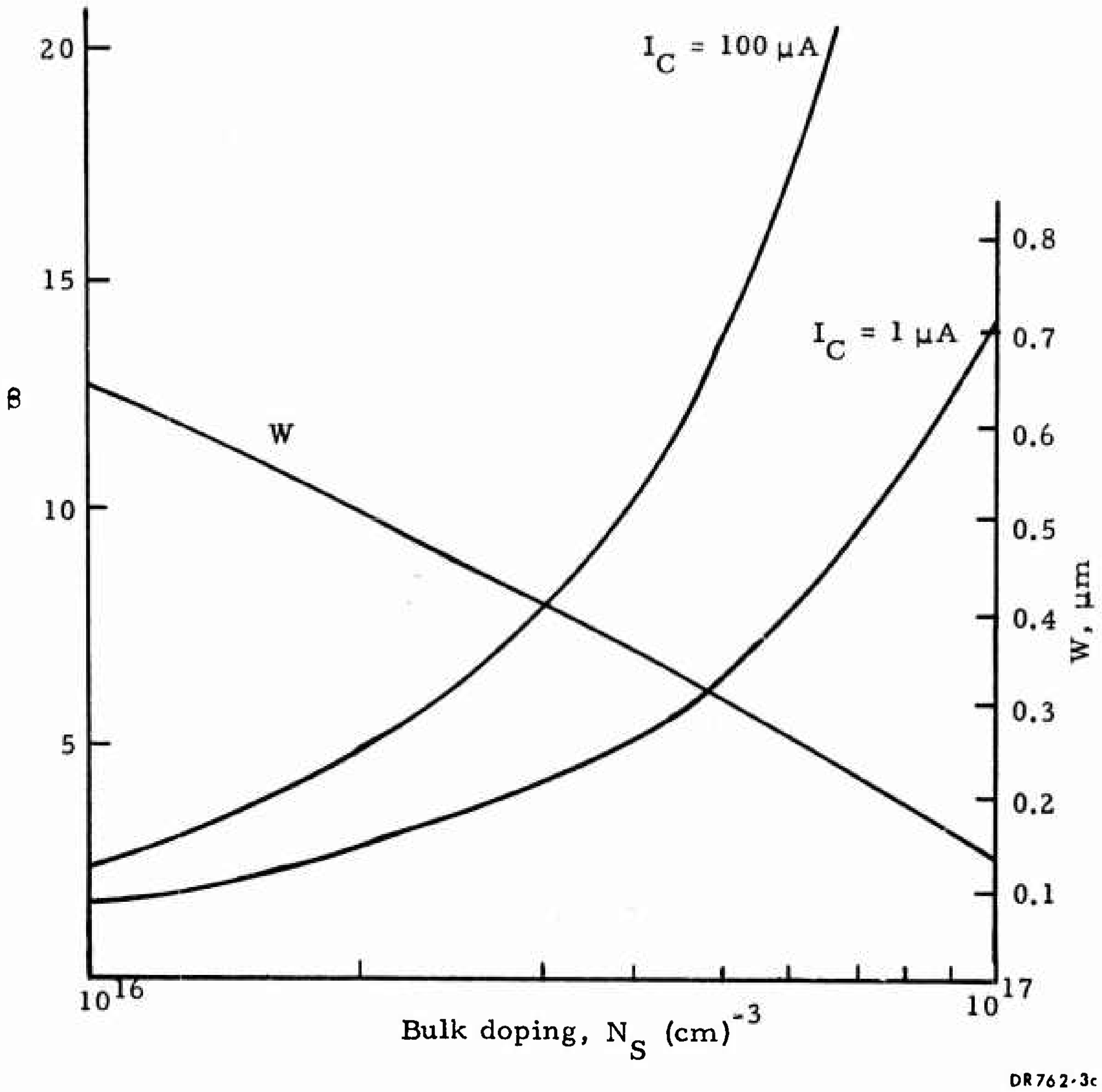

Figure 2-9. Variation of npn basewidth, W, and current gain, β, with bulk substrate doping, N_S, for two values of collector current, I_C, for a fixed base drive-in $Dt = 1.96 \times 10^{-9}$ cm^2 and fixed base surface concentration of 2×10^{18} cm^{-3}.

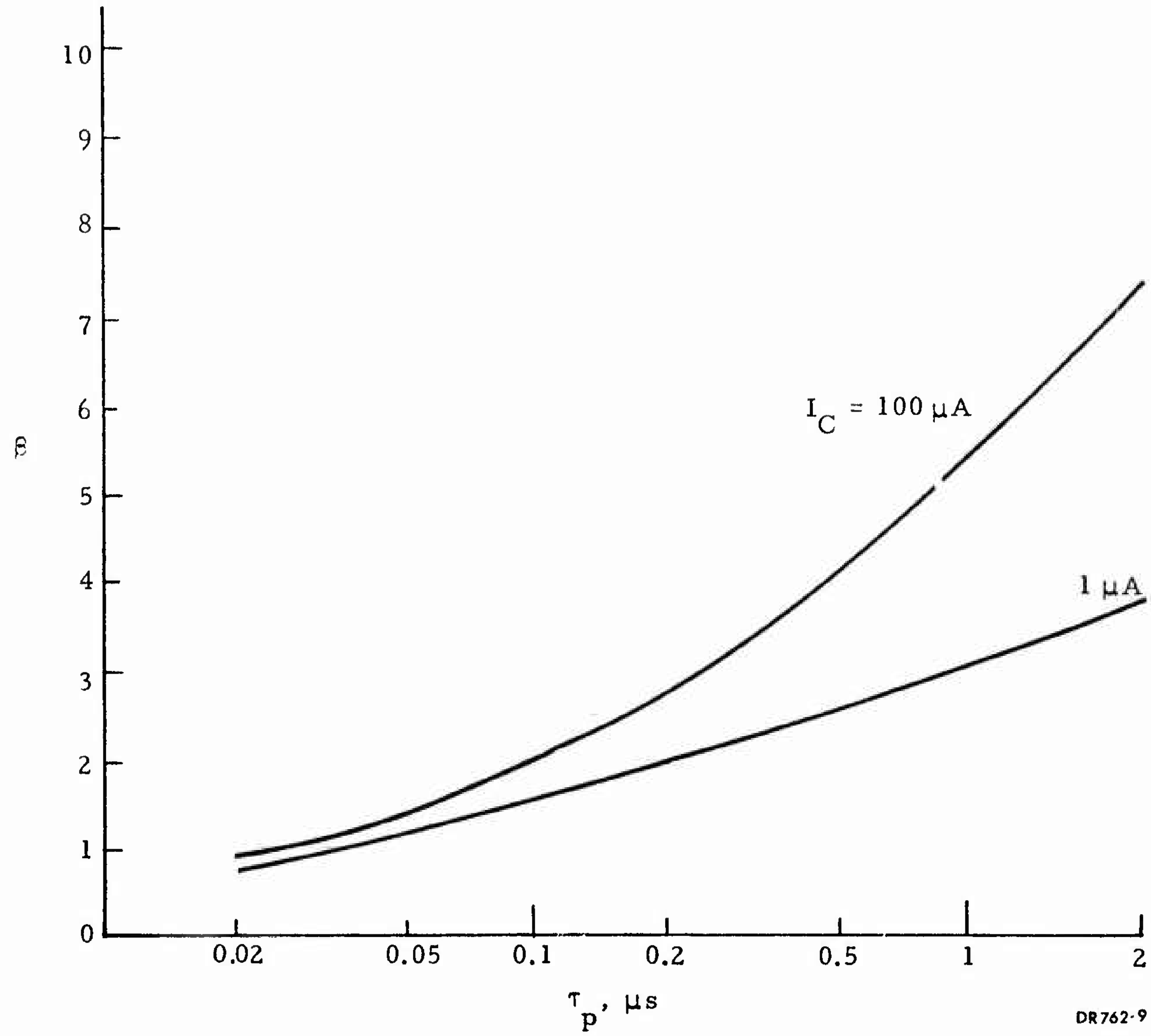

Figure 2-10. Npn current gain, β, versus lifetime for holes in bulk substrate, τ_p, for two values of collector current.

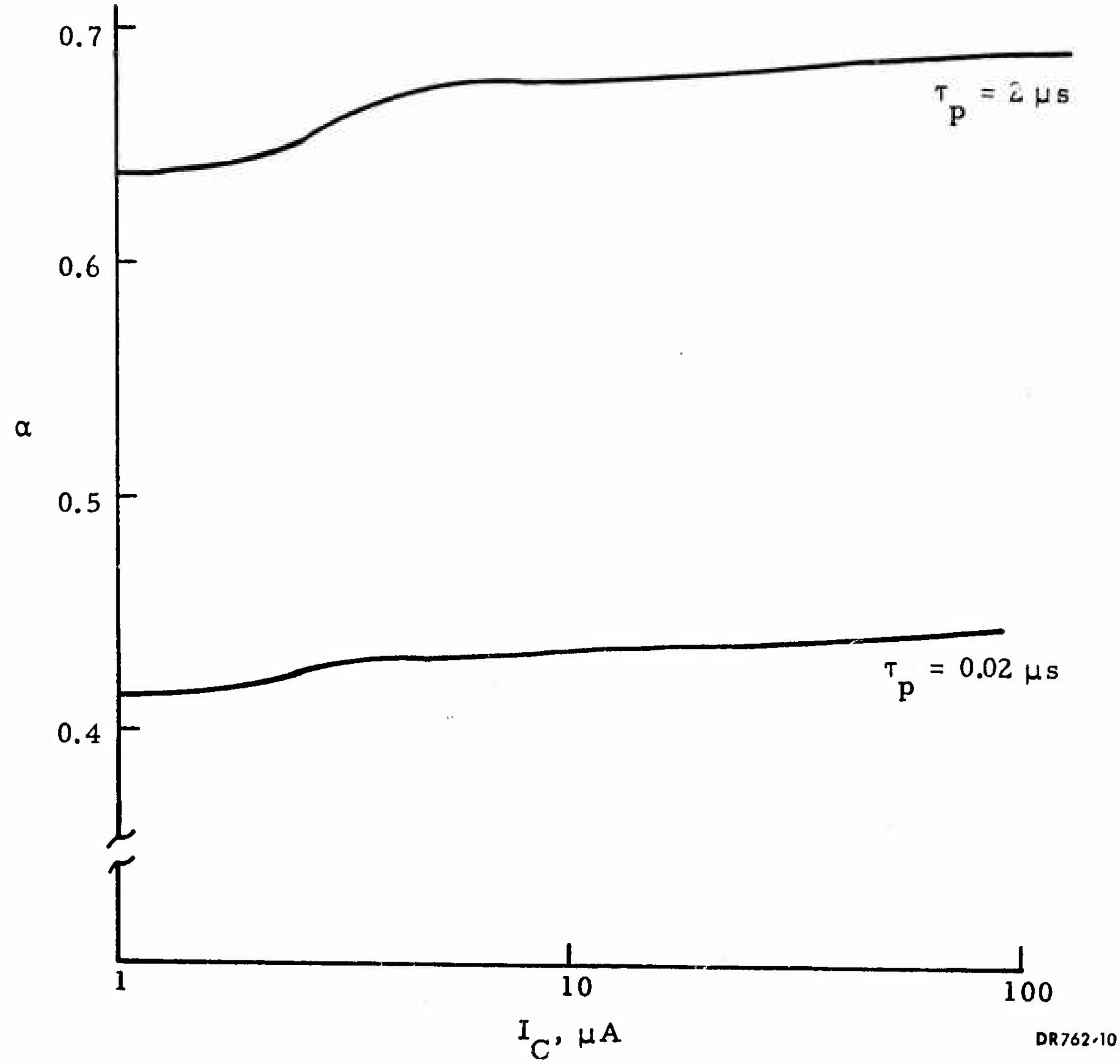

Figure 2-11. Pnp current gain, α, versus collector current, I_C, for two values of hole lifetime in bulk substrate, τ_p.

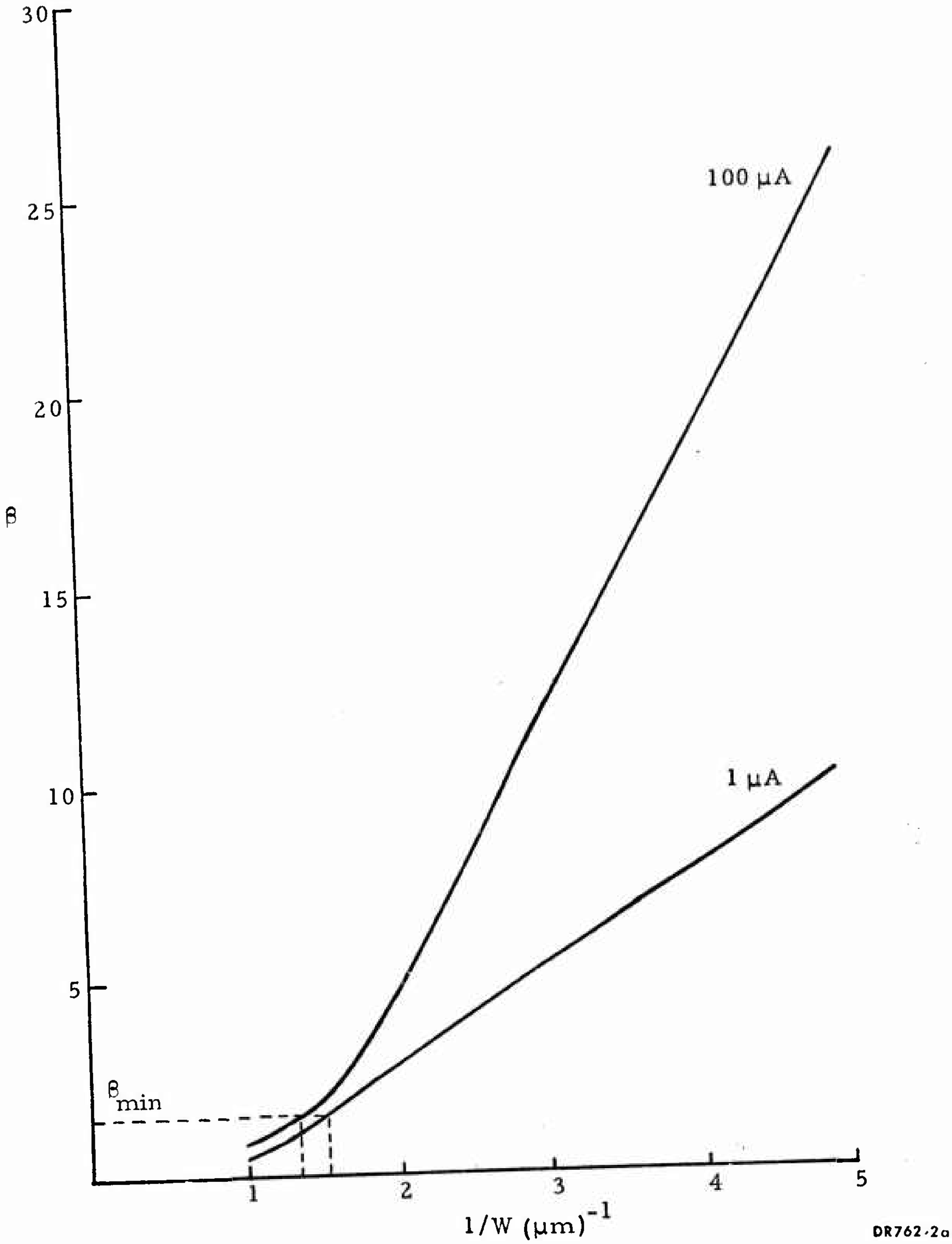

Figure 2-12. Variation in npn current gain, β, with reciprocal of base width, 1/W, for two values of collector current. Base surface concentration is $2 \times 10^{18}\ cm^{-3}$ and substrate doping is $10^{16} cm^{-3}$.

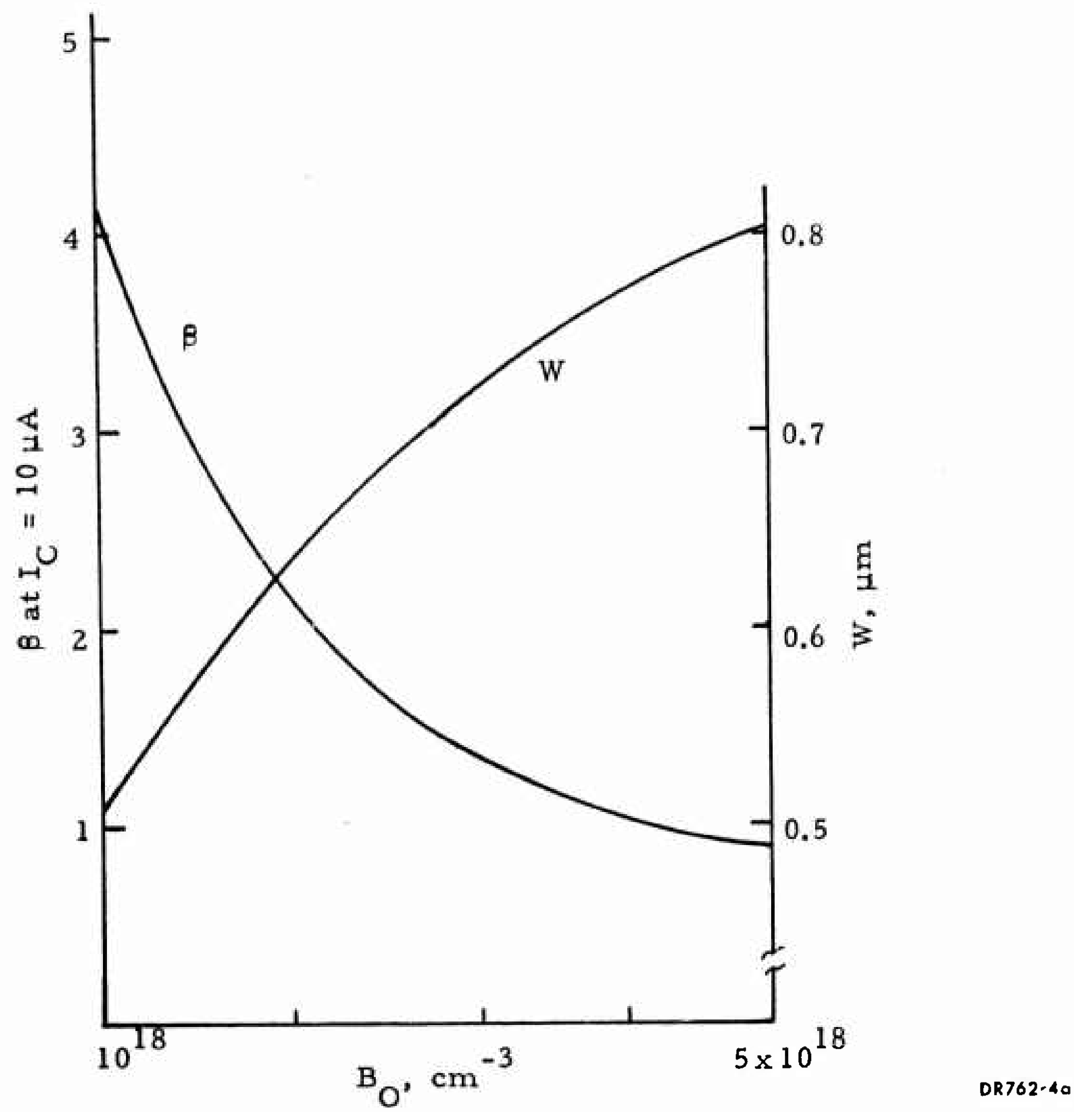

Figure 2-13. Npn current gain, β, and basewidth, W, versus base surface concentration, B_O, for a fixed base diffusion Dt = 1.96×10^{-9} cm^2 and fixed bulk substrate doping of 10^{16} cm^{-3}.

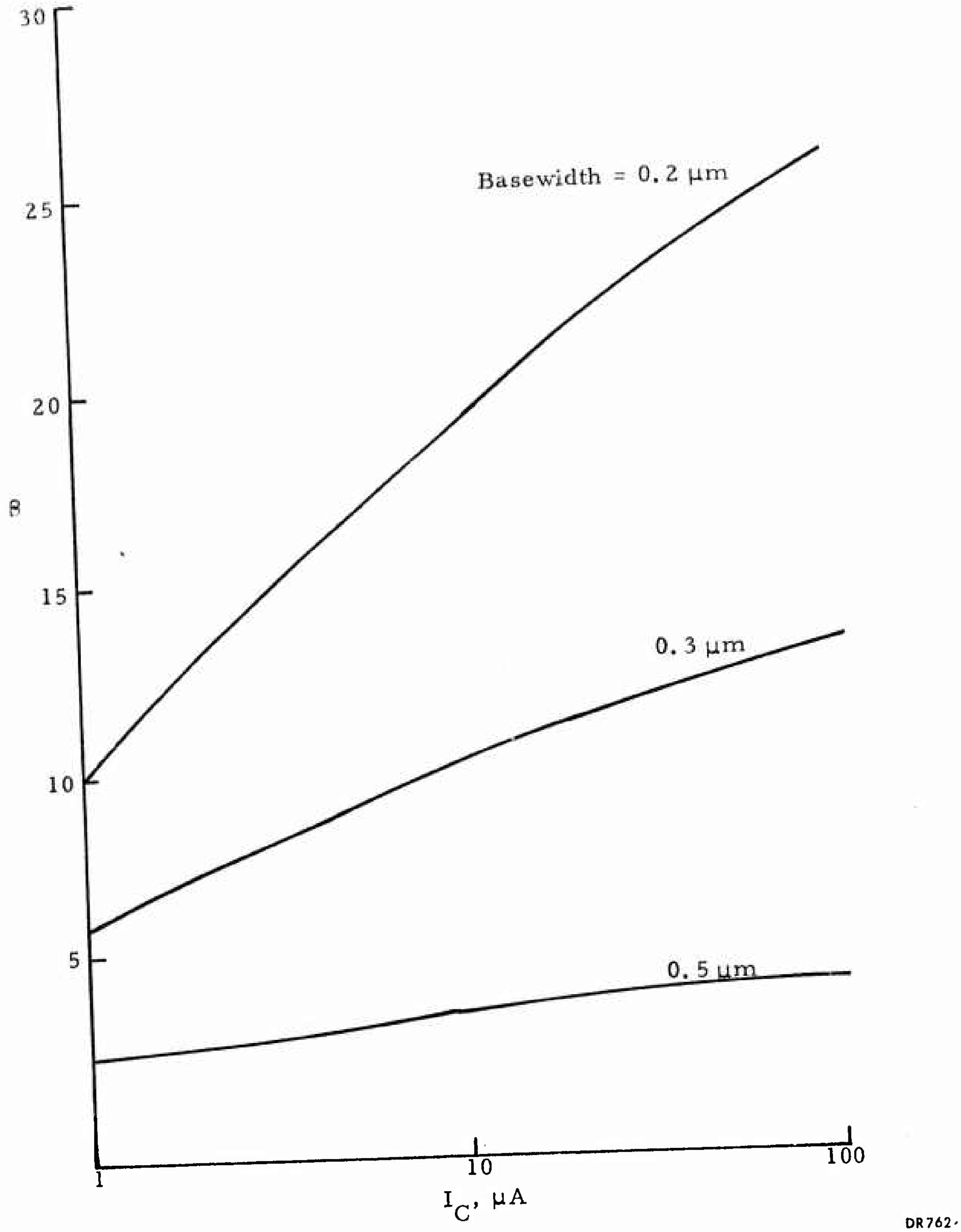

Figure 2-14. Npn current gain, ß, versus collector current, I_C, for three values of basewidth. Base surface concentration is 2×10^{18} cm^{-3} and substrate doping is 10^{16} cm^{-3}.

SECTION 3

I^2L PROCESS DESIGN

The I^2L processing activity has been directed toward maintenance of the standard process, as well as to application of selective modifications to achieve improved performance without undue process complexity. Experimental comparison is made between the modified processes and the standard process as a baseline to determine performance vs yield trade-offs.

This section describes the most recent development of the I^2L process technology at NRTC. Emphasis in I^2L process development is placed on increasing circuit performance primarily by making improvements in transistor design. The process steps given and the advantages obtained are presented.

3.1 STANDARD PROCESS DESCRIPTION

Since I^2L is a bipolar integrated-circuit technology, the common semiconductor wafer processing practices are generally used for both topological and structural designs. Figure 3-1 shows a cross section of basic I^2L cell. The latter is a multicollector npn transistor with a pnp current source. The p-type diffusion forms the emitter (injector) and collector of the lateral pnp as well as the base of the npn. The pnp base and the npn emitter share the common semiconductor volume (n-epitaxial layer).

The starting material used in fabricating the above I^2L cell is an n-type epitaxial layer on an n+ silicon substrate with a nominal epi thickness of 3-5 μm and resistivity of 0.1 to 0.3 ohm-cm. The fabrication steps are listed below:

(1) Initial oxidation with HCl-steam

(2) Define injector and base

(3) Deposit boron with boron nitride

(4) Drive-in boron; 250 ohm/sq, x_j = 1.5 μm

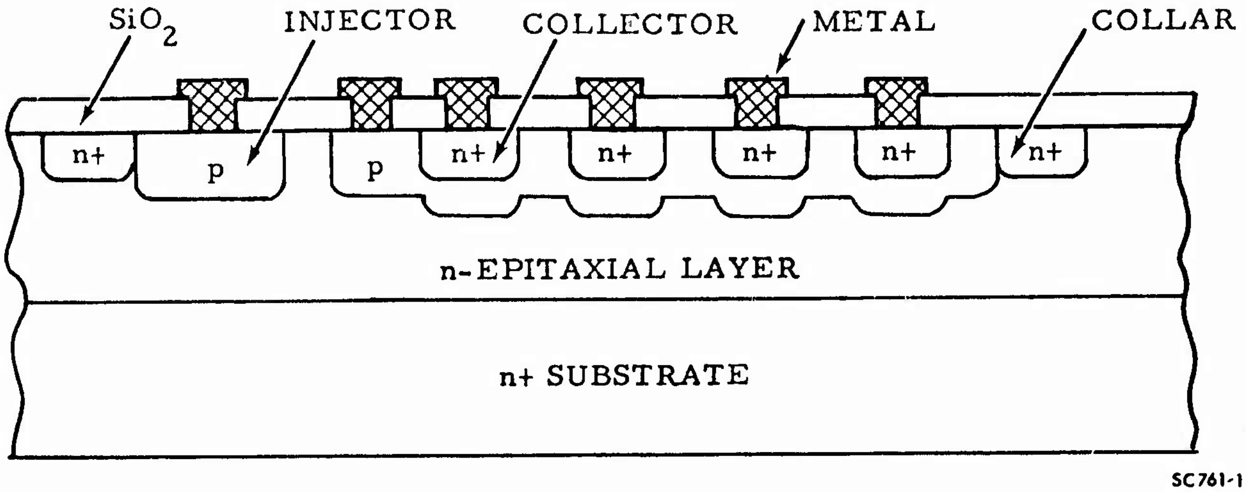

Figure 3-1. Standard epitaxial I^2L structure.

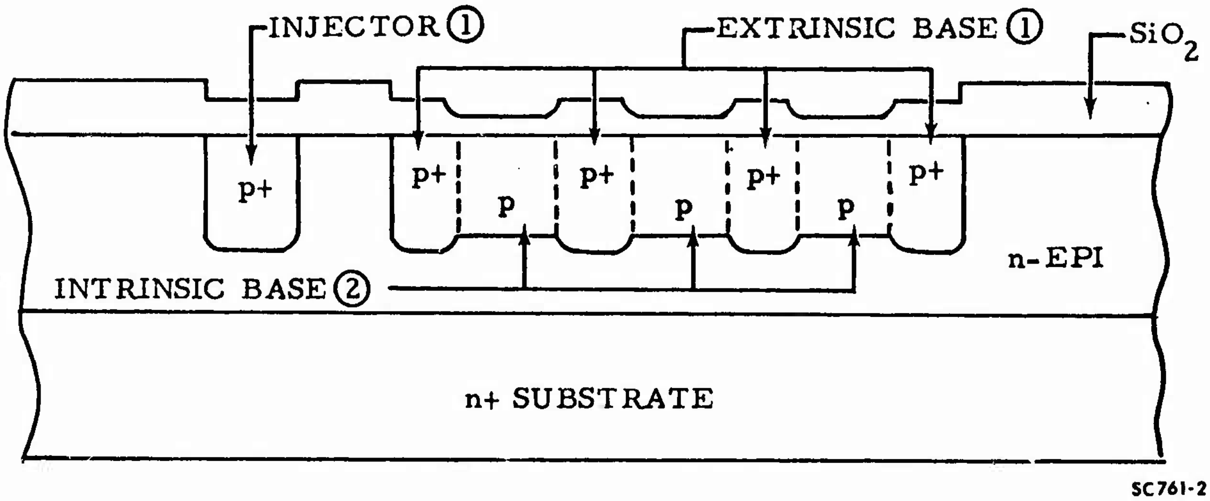

Figure 3-2. Horseshoe I^2L structure.

(5) Define n+ collar and collector

(6) Deposit phosphorus - $POCl_3$ process

(7) Drive-in phosphorus; 10 ohm/sq, $x_j \geq 1\ \mu m$

(8) Open contact hole

(9) Aluminum metallization

(10) Define aluminum

(11) Sinter contacts

It is noted that such a process contains only two diffusion cycles and single-level metallization. Hence, process complexity is comparable to the standard NMOS process that utilizes both phosphorus diffusion and threshold-voltage adjustment by ion implantation.

For circuits where speed performance is not crucial, lower cost I^2L chips can be fabricated with bulk silicon. Therefore, an investigation is underway to apply this bulk approach to low- and moderate-performance military requirements. The bulk substrate used in this work has a resistivity in the range of 0.1 - 0.3Ω-cm. Since diffusion is performed from the top surface, the npn device is formed on a relatively lightly-doped emitter. In this inverse mode of operation, hole injection into the emitter region generally controls the npn current gain as well as the logic gate fanout.

3.2 ALTERNATIVE PROCESS STEPS

The options for alternative process steps exploits the double diffused base or "horseshoe" base process which was reduced to practice during 1975 as part of the NRTC company funded I^2L project. This base structure, shown in Figure 3-2, is fabricated in two steps:

(1) A higher boron concentration is used to form both the injector and the extrinsic base (outside collector region) of the npn device

prevent surface inversion and to increase the lateral pnp injection efficiency.

(2) A comparable lower boron concentration is formed in the intrinsic base region below the collector.

The two-level base diffusion practically eliminates the base push-out effect which usually occurs when phosphorus is diffused into a boron-diffused base region. The new modified process presented here should result in lower cost, higher yield and better performance. Also, it will allow fabrication of Schottky barrier diodes by implanting a buried p-layer into the intrinsic base regions. This technology will be discussed in the next section.

Electrical characteristics of the standard and "horseshoe" I^2L process are summarized in Table 3-1 below. In NRTC's modified process, the doping level in the intrinsic base is slightly lower than for conventional I^2L. The process results in higher npn and pnp collector currents and higher current gains. The minimum delay and delay-power product can also be improved.

TABLE 3-1. I^2L TRANSISTOR PERFORMANCE

Process	α	β
Standard I^2L (epi)	0.5-0.6	5-10
"Horseshoe" I^2L (epi)	0.6-0.7	10-20
Nonepitaxial I^2L	0.3-0.5	2.5-5

In short, NRTC's "horseshoe" is believed to have considerable advantage in a standard I^2L structure. By virtue of its process flexibility and its simple basic design concepts, it offers considerable promise for optimazation of the current gain of the npn and pnp devices while simultaneously improving delay-power product.

3.3 ADVANCED PROCESS TECHNOLOGY

Because of rapid development in large-scale integration, I^2L will be used in a wide range of new circuits and in combination with other LSI technologies such as TTL, ECL, and bipolar linear to form a mixed bipolar LSI family. The original development of I^2L emphasized a favorable delay-power product rather than high speed operation. To interface I^2L with other LSI technologies, refinements are underway at NRTC to investigate increasing the L^2L speed to approach that of standard low-power Schottky TTL.

To develop an I^2L process technology yielding higher speeds and low power consumption, it is necessary to review both physical and electrical factors which affect the characteristics of the typical delay-power product performance. In the constart delay-power region of the curve, the propagation delays are controlled by the depletion capacitance of the npn device. Under the present study at NRTC, there are, at least, two modified structures which will further reduce the delay-power product:

Firstly, a boron-implanted intrinsic base region in the NRTC "horseshoe" structure instead of the conventional chemical diffusion is being considered. In an implanted npn device, it is possible to fabricate a narrower base width with a lower base impurity doping which will result in a higher β.

The process steps in fabricating the implanted npn into the NRTC "horseshoe" structure, shown in Figure 3-3, are carried out as follows:

(1) Initial oxidation with HCl-steam
(2) Define the extrinsic base and injector
(3) Deposit boron
(4) Drive-in boron
(5) Define the intrinsic base
(6) Regrow 1000 Å oxide on the base window

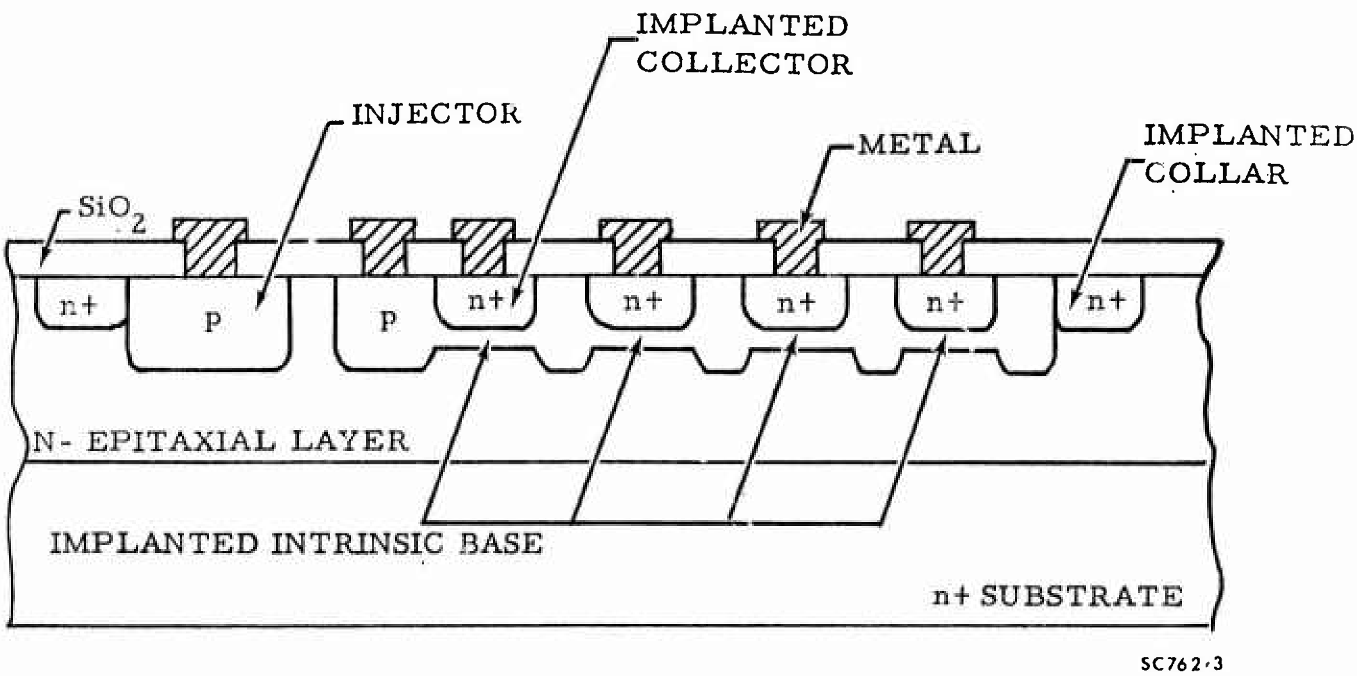

Figure 3-3. Implanted I^2L horseshoe structure.

(7) Implant boron

(8) Drive-in boron

(9) Define n+ collar and collector

(10) Regrow 1000 Å oxide on n+ windows

(11) Implant phosphorus

(12) Drive-in phosphorus

(13) Open contact

(14) Metallization.

It is generally known that the delay-power product can be decreased by reducing the emitter area of the basic gate. In using the layout rule based on minimal dimensions of 5 μm instead of 10 μm, the speed-power product can be decreased from the range 1 to 2 pJ/gate to about 0.25 to 0.5 pJ/gate.

The second structural modification for improvement in delay-power product is the integration of Schottky barrier diodes at the I^2L npn collectors. By implanting boron at high energies into the intrinsic base region, a "p" type buried layer can be achieved, with the surface concentration virtually unchanged. This approach requires relatively high energies or the use of doubly charged boron (B++) ions. The annealing of the implanted boron can be done at relatively low temperatures which minimizes the lateral spreading of the Gaussian profile. A cross-section of the ion-implanted Schottky barrier process is shown in Figure 3-4.

Fabricating steps are outlined as follows:

(1) Initial oxidation with HCl-steam

(2) Define the extrinsic base and injector

(3) Deposit boron

(4) Drive-in boron

(5) Define the shallow collar

(6) Deposit phosphorus

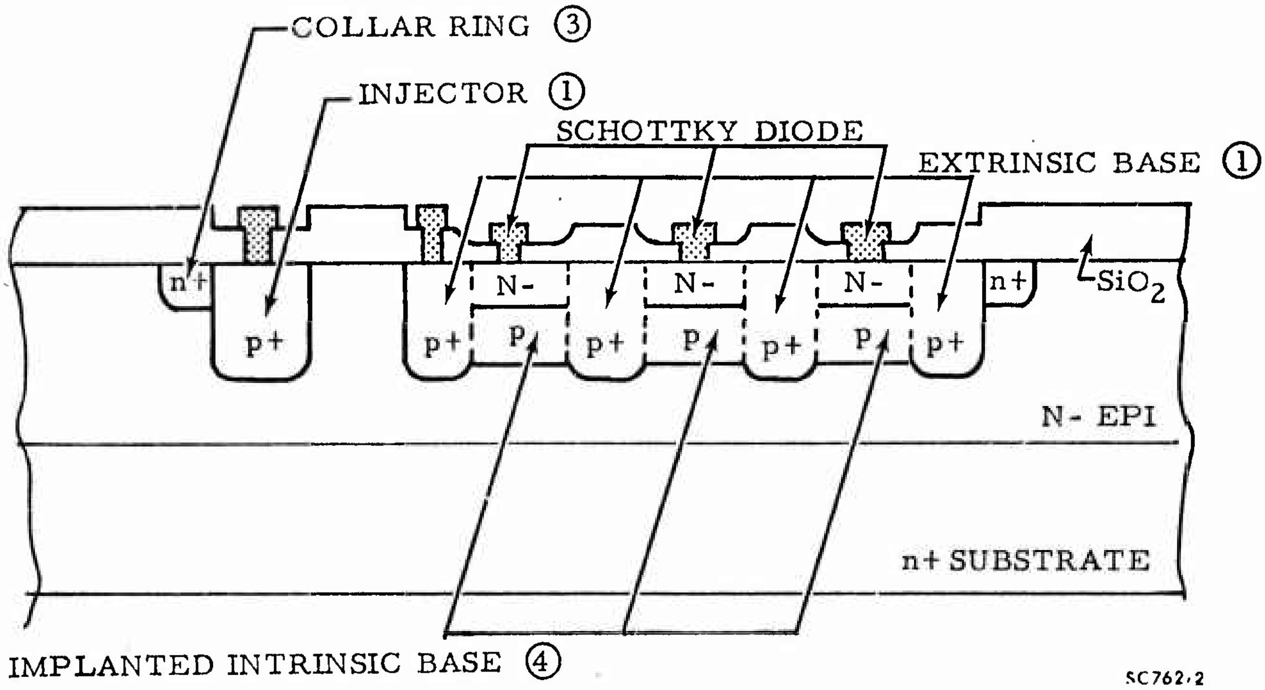

Figure 3-4. Horseshoe I^2L structure with Schottky collectors.

(7) Drive-in phosphorus

(8) Define the intrinsic base

(9) Regrow 1000 Å oxide on the window

(10) Implant boron

(11) Anneal boron implant

(12) Open contact

(13) Metallization.

The primary limitation in this approach is obtaining the required implant energy. An alternative process that should be investigated is to ion-implant both boron and arsenic species, and subsequently drive these impurities to achieve the desired profile. The simultaneous drive-in of arsenic and boron impurities appears to permit the realization of narrow-base transistors. This results from a reduction in the difference between the two diffusion constants under conditions of simultaneous drive-in.[3]

3. Richard B. Fair and Paul N. Pappas, Journal of ECS, 1241 (1975).

SECTION 4

I^2L TEST CHIP CIRCUIT DESIGN

The purpose of the test chip is twofold:

(1) To verify the device model parameters used for circuit design and analysis, and

(2) To determine the limits of circuit performance parameters as functions of layout, wafer process, and circuit design variables.

As a result, almost all experiments included within the test chip are directly related to these two objectives, although a few devices are included for process monitoring. The information obtained in the evaluation of the test chip will be utilized in the design of the 6 x 128 shift register array, as required in the second half of the contract.

4.1 MODEL-VERIFICATION DEVICES AND CIRCUITRY

The parameters necessary to adequately model I^2L devices primarily involve those that control the npn and pnp current gains, and the variables that control switching response parameters including delay-power product and the minimum propagation delay time. Several I^2L devices of various geometries are included to verify dc model parameters. In addition, parameters that control switching response will be studied primarily with the use of ring oscillator circuitry of various designs. Ring oscillators with single as well as multiple collectors are included. The effect of the n+ collar in hole injection and emitter-base capacitance will likewise be evaluated with an oscillator design containing a 10 μm separation between the collar and the base diffusion. Ring oscillators are very convenient for measurements made using a wafer test probe station because the stray wiring capacitance does not load the oscillator loop, since the output is monitored from a separate device. As a result, an accurate measurement of the period of oscillation and consequently the inverter propagation delay is obtained.

To supplement this ring oscillator measurement, a serial inverter propagation delay chain is included on the test chip. This experiment contains many stages of delay, and the differential time delay introduced by the several inverter stages is sensed by an "exclusive OR" gate. The schematic for this circuit is shown in Figure 4-1, with the timing diagram shown in Figure 4-2. The "exclusive OR" gate functions to detect the time interval during which the inputs A and B are unequal. This interval is a direct measure of the delay through the number of stages, as indicated on the timing diagram.

4.2 I^2L FUNCTIONAL CIRCUITRY

The functional circuitry on the test chip will aid in the determination of the performance limits of medium scale size arrays. In addition, the MSI arrays will be used to predict performance of LSI complexity devices, prior to the fabrication of the 6 x 128 register array to be developed during the second half of the contract.

The MSI functional circuitry consists of 3-bit binary counters and 32-bit serial shift registers. Both circuits use a conventional I^2L edge triggered D-type flip-flop. A logic diagram of this flip-flop is shown in Figure 4-3 using NAND logic; a circuit schematic is given in Figure 4-4. As shown in Figure 4-3 the output latch consists of cross-coupled gates G6 and G7 functions as a NAND SR flip-flop, with the input condition $\overline{S} = \overline{R} = 1$ resulting in no output change. Notice that this occurs whenever the clock line is high, which forces the outputs of G4 and G5 high, and the Q and $\overline{Q}$ outputs remain at the previous state. When the negative transition occurs on the clock line, this permits the steering gates, G1 through G5, to generate the appropriate values of $\overline{S}$ and $\overline{R}$ as functions of the data line. In other words, the data line (D) is sampled at the negative transition of the clock, and the Q and $\overline{Q}$ outputs assume the corresponding values. Observe that the clock and data lines on the flip-flop are completely isolated, thus providing a good clock noise margin.

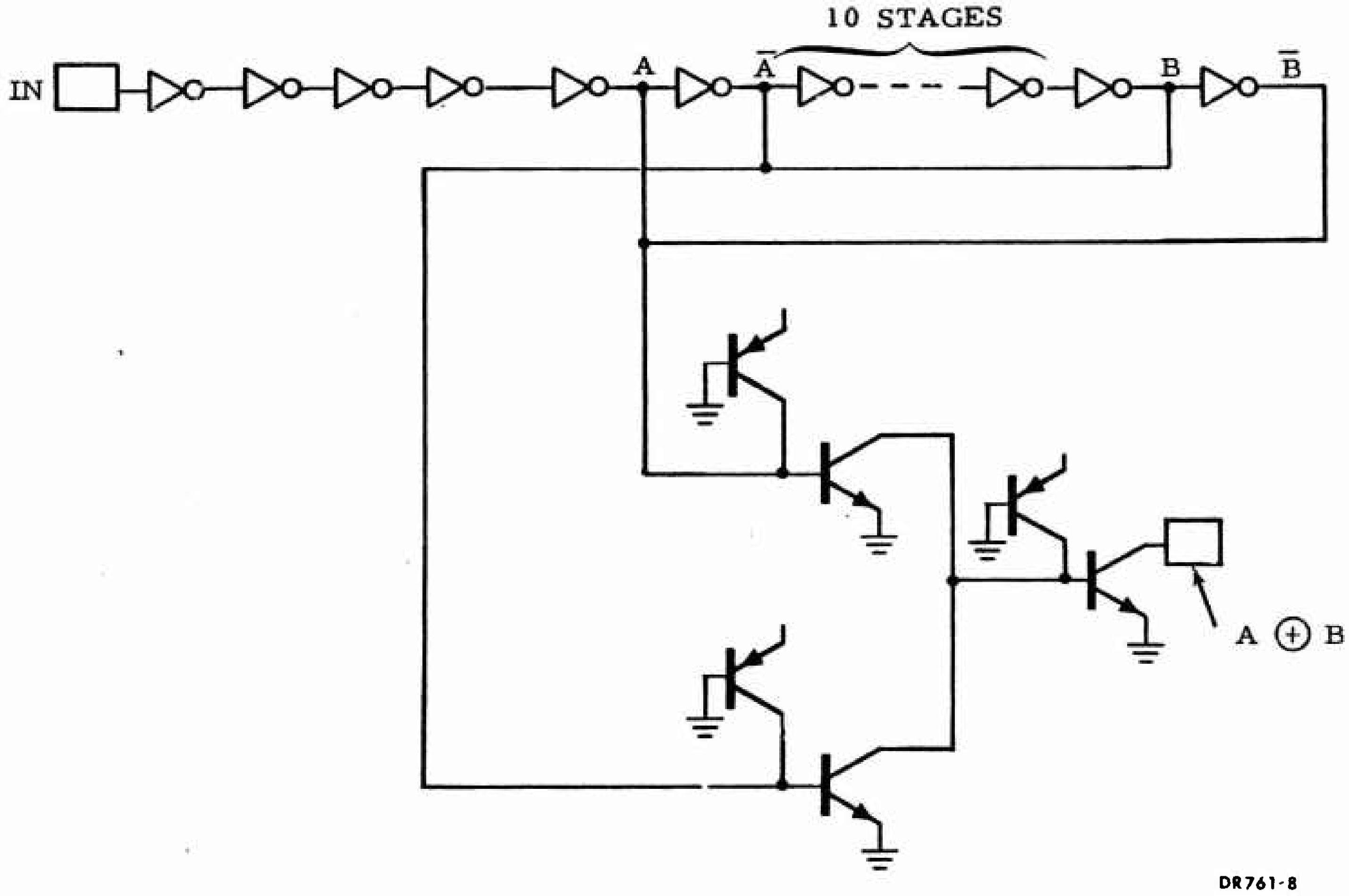

Figure 4-1. Schematic of I^2L propagation delay test circuit.

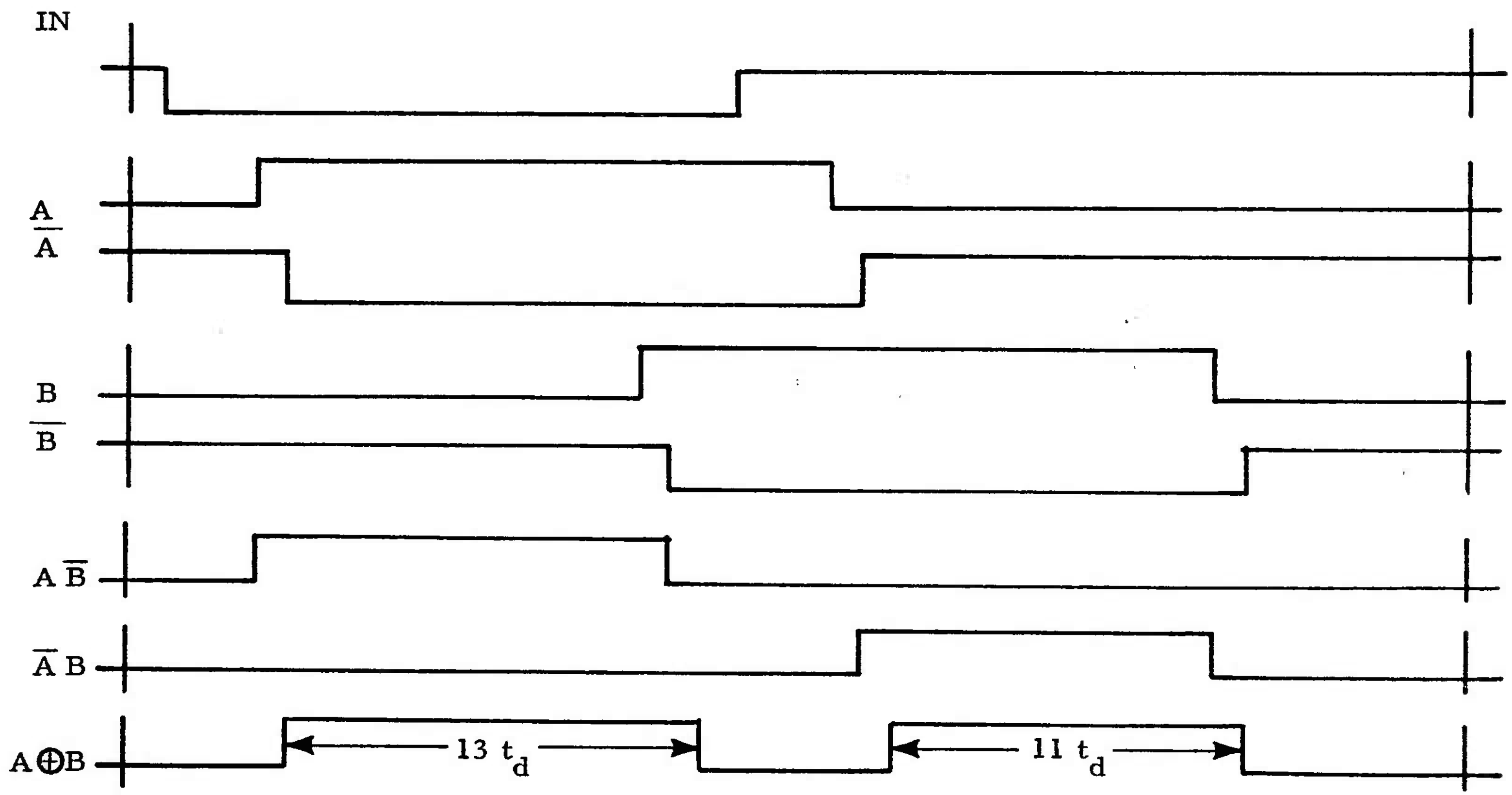

Figure 4-2. Timing diagram of I^2L inverter propagation delay test device.

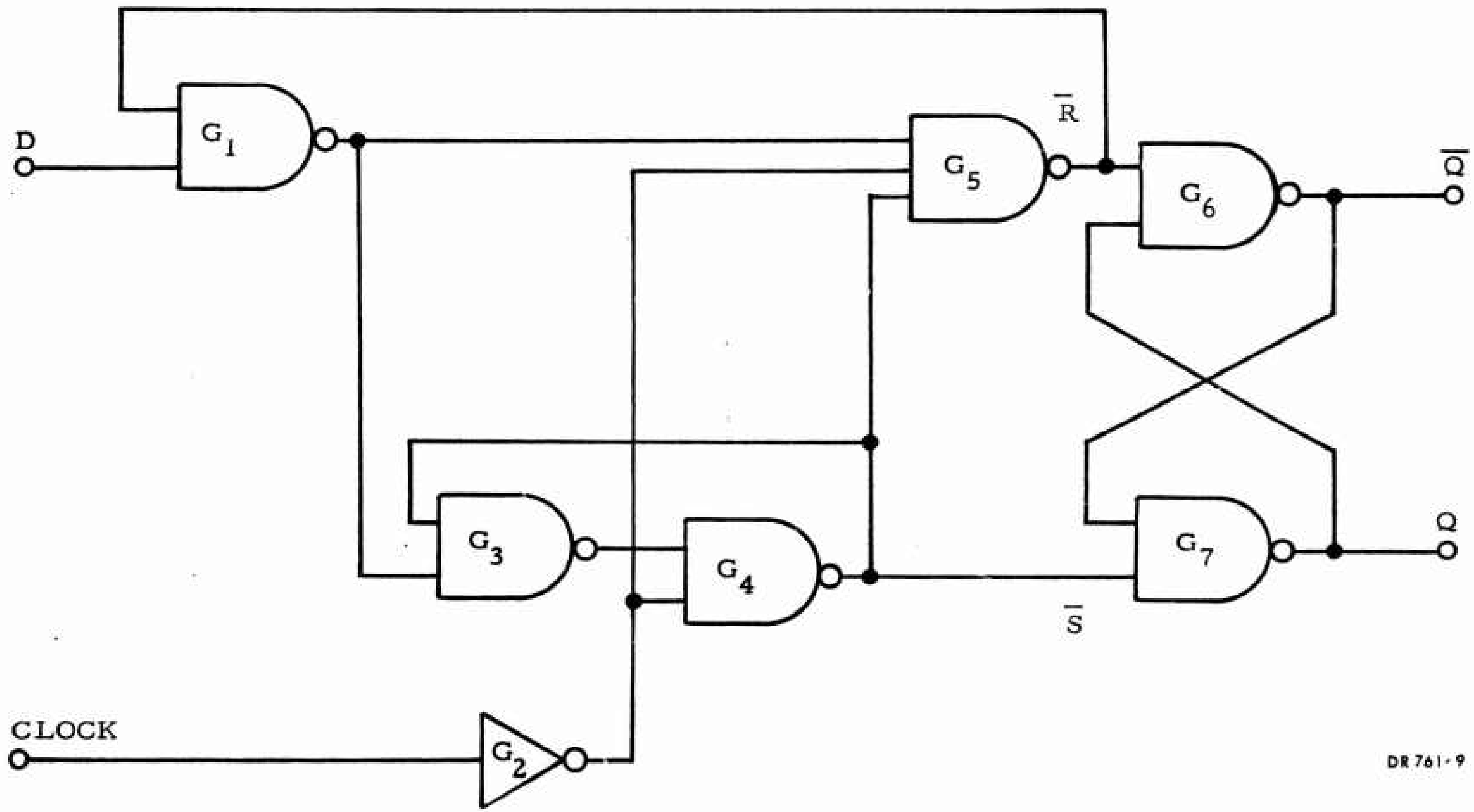

Figure 4-3. Logic diagram of D-type flip-flop.

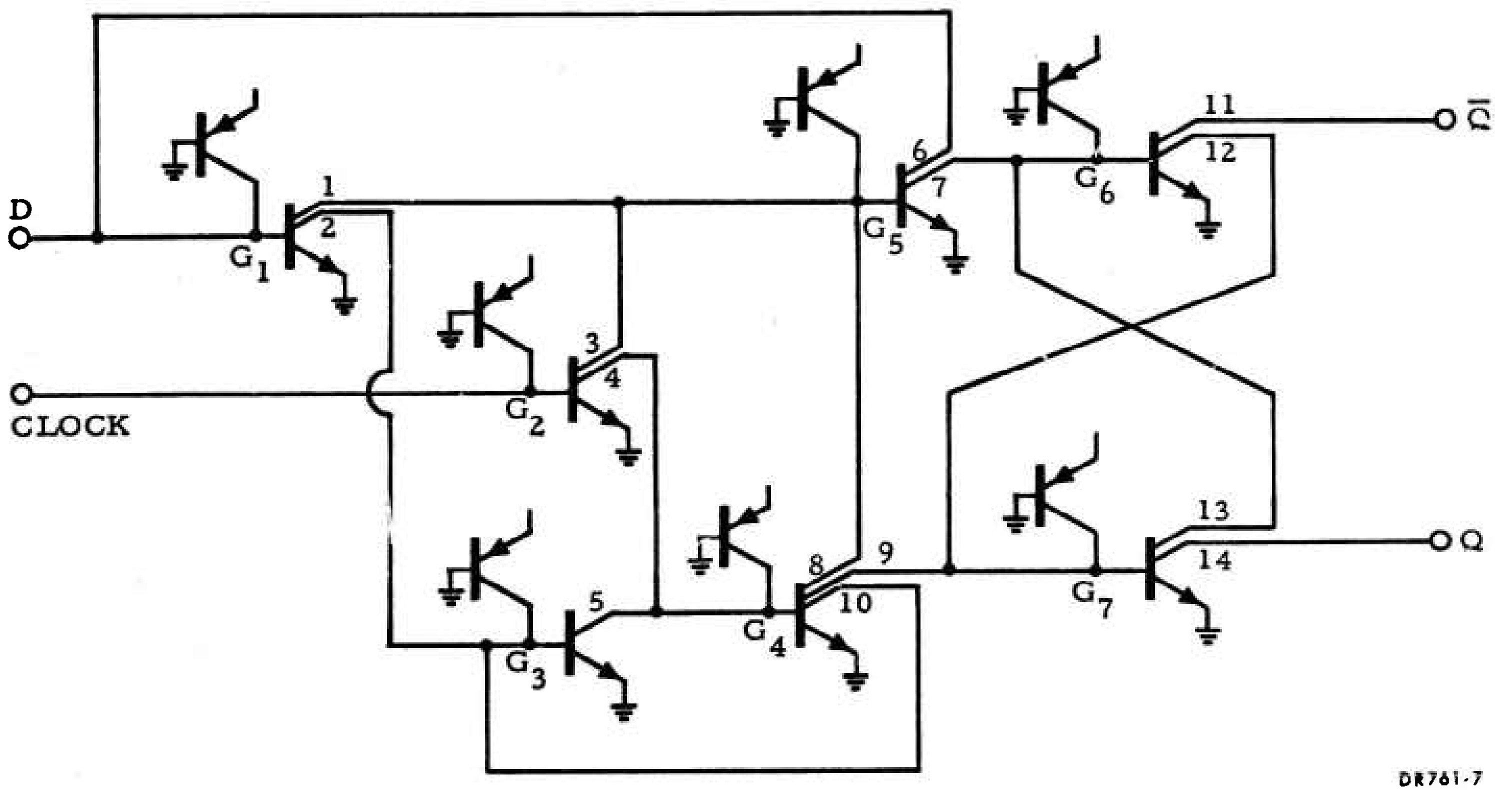

Figure 4-4. Circuit schematic of an I^2L D-type flip-flop.

4.2.1 Three-Bit Counters

Three-bit binary counters, containing the negative edge-triggered D-flip-flops and steering logic, were designed. A schematic of the counter is shown in Figure 4-5, in which only the input and output terminals of the flip-flops are indicated with the steering logic fully indicated. This design is a conventional synchronous counter (i.e., all flip-flops change state simultaneously with the negative edge of the clock), with a ripple carry. The advantage of this approach is that the counter length can be expanded with no increase in the fanout requirement of the steering logic. Because the maximum fanout required is equal to 3 for the flip-flop and two for the steering logic, the wafer yield is anticipated to be good.

4.2.2 Serial Shift Registers

Serial shift registers, 32 bits in length, are included on the test chip to evaluate performance and yield prior to the design of the 6 x 128-bit register array. The test chip registers contain 32 flip-flops identical to those included on the 3-bit binary counter. A common clock line is used to guarantee synchronous operation. Due to the large number of contact holes and intracell metal wiring, the shift register yield per unit area will be representative of a complex logic array.

4.2.3 Input Buffer Circuitry

Input buffer circuitry has been included as an integral part of the counter and shift register circuitry. Figure 4-6 shows the schematic of the input npn transistor, Q_I, interfacing with a typical I^2L input. The function of the npn is to provide isolation between the low capacitance I^2L npn base and the larger stray capacitance of the external circuitry. This approach permits the rise time of the input to be minimized as a function of injection level. The time constant of the external circuitry, typically an open collector TTL gate, can be optimized by the choice of the pull-up resistor. For typical values of external circuit capacitance, the value of this pull-up resistor will be sufficiently large to avoid excessive storage time of the npn input transistor Q_I.

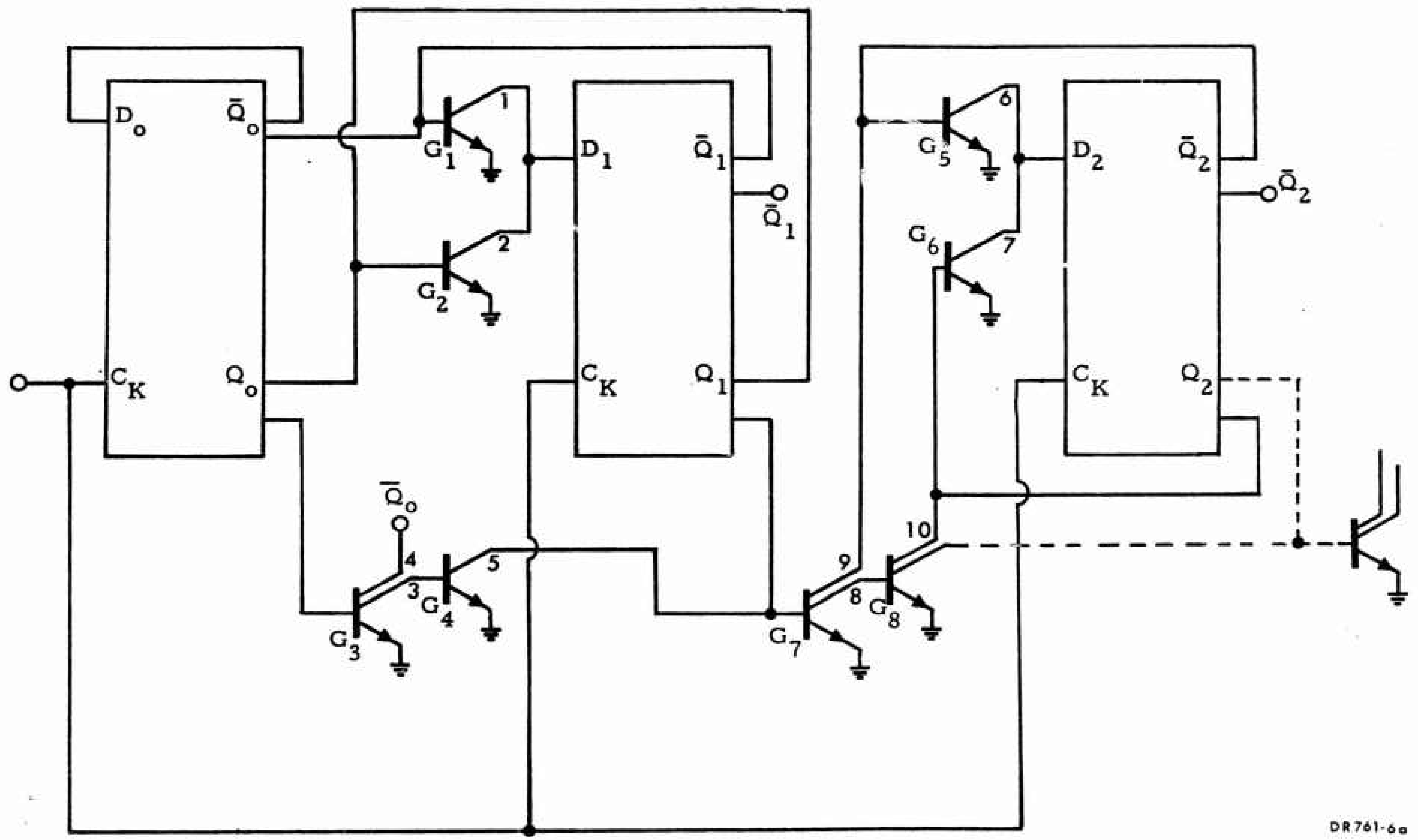

Figure 4-5. I^2L three-bit binary counter schematic.

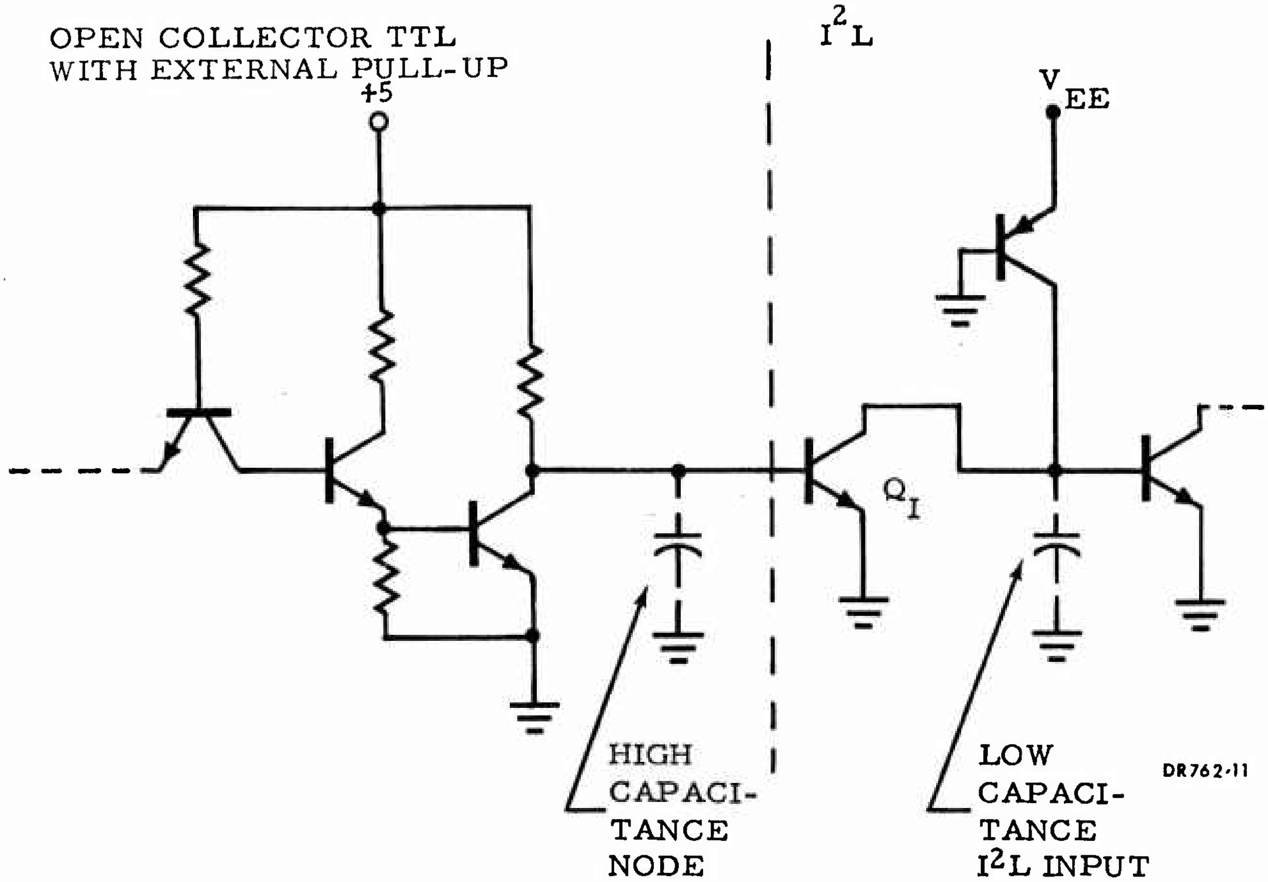

Figure 4-6. I^2L input buffer transistor, Q_I, interfacing with TTL.

4.2.4 Output Buffer Circuitry

Output buffer circuitry is required to increase the current drive of an I^2L gate. Typically, I^2L gates operate in the range of $1\mu A$ to $100\mu A$ for optimum delay-power product. Hence, it is necessary to increase the current drive by a factor of 10 to interface directly with low-power TTL. As discussed previously, the current gain of an npn transistor increases with the collector-to-emitter area ratio (S_C/S_E). Then the required gain of the npn can be achieved by proper adjustment of S_C/S_E. This is the approach that was taken in the design of the output buffer shown in Figure 4-7. An external pull-up resistor is used with this buffer to provide the source current, while the output npn is capable of sinking one TTL/LS load over the normal range in injection level.

4.3 FUNCTIONAL CIRCUIT LAYOUT VARIATIONS

Two types of layout design rules were incorporated into the test chip. This will permit performance vs. yield tradeoffs to be identified during the test chip evaluation. The tighter design rules consist of a $5\mu m$ minimum oxide cut and spacing (type A rules) whereas the relaxed rules (type B) call for $7.5\mu m$ minimums. Table 4-1 summarizes the design rule parameters that limit circuit packing density for both type A and type B rules.

To make a direct comparison between the performance of the two design rules, special use of the automated graphics system was made. The functional circuit layouts were completed at 1000 X scale using the relaxed rules. Then these layouts were scaled down by the ratio of (5/7.5) using the graphics system capability. Spacing factors such as pnp basewidth and collector-to-collar were likewise reduced. The resulting layouts were then made available consistent with either type A or type B rules. In general, the linear dimensions of the gates were scaled by the ratio (5/7.5) and the area was scaled by a factor of $(5/7.5)^2$. The test chip includes the following variations in design rules and injector layout, indicated in Table 4-2.

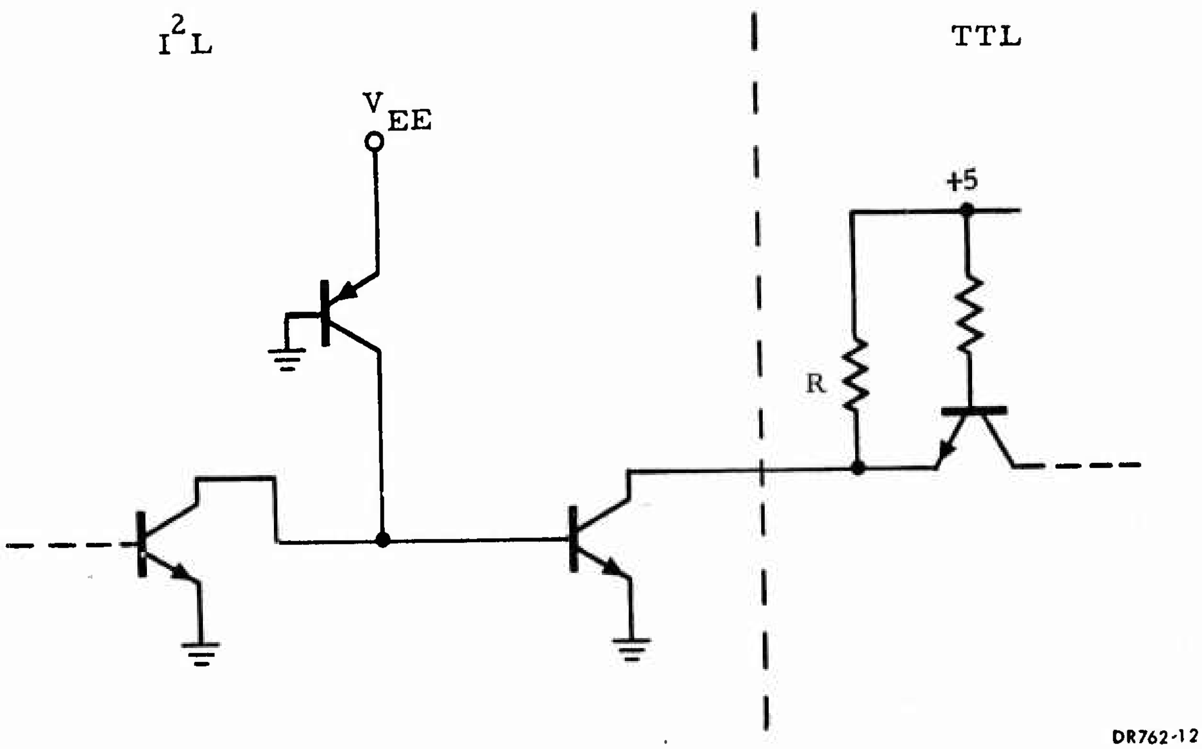

Figure 4-7. I^2L output buffer shown with external pull-up resistor, R, driving TTL gate.

TABLE 4-1. LAYOUT DESIGN PARAMETERS THAT LIMIT LSI PACKING DENSITY

Layout Parameter	Type A Rules	Type B Rules
Oxide Cut	5 μm x 5 μm	7.5 μm x 7.5 μm
Oxide Cut Spacing	5 μm	7.5 μm
Metal Line Width	7 μm	10 μm
Metal Line Spacing	5 μm	7.5 μm
Maximum Metal Lines/mm	~80	~60

TABLE 4-2. TEST CHIP LAYOUT VARIATIONS

3 Bit Binary Counter Variations	
Parallel Injectors Perpendicular Injectors	Type A Rules
Parallel Injectors Perpendicular Injectors	Type B Rules

32-Bit Shift Register Variations	
Perpendicular Injectors	• Type A Rules • Type B Rules

4.4 DC DESIGN PARAMETERS OF I^2L LOGIC GATES

The design of I^2L logic gates requires reasonably accurate circuit models in order to calculate important dc parameters, including input transition voltage, noise margin, and power dissipation. Figure 4-8 contains a circuit schematic for the I^2L inverter, and the design equations can be applied to multi-collector logic gates as well as an inverter.

Bipolar transistor collector current varies with applied base voltage in the active region and with base voltage as well as collector voltage in the saturation region. As a result, a summation of currents at the npn base will provide a solution for the inverter output voltage as a function of its input voltage. With reference to Figure 4-8, the currents are summed at node 1 as follows:

$$I_1 = I_2 + I_3 \tag{4-1}$$

where I_1 = pnp collector current

I_2 = npn collector current from preceeding inverter

I_3 = npn base current

It is necessary to write the collector and base currents in terms of:

- semiconductor material parameters
- wafer process parameters
- transistor geometries

From basic semiconductor physics, and neglecting the saturation currents in comparison to the foreward currents,

$$I_1 = I_{PO}\left[\exp\left(qV_{EE}/kT\right) - \exp\left(qV_o/kT\right)\right] \tag{4-2}$$

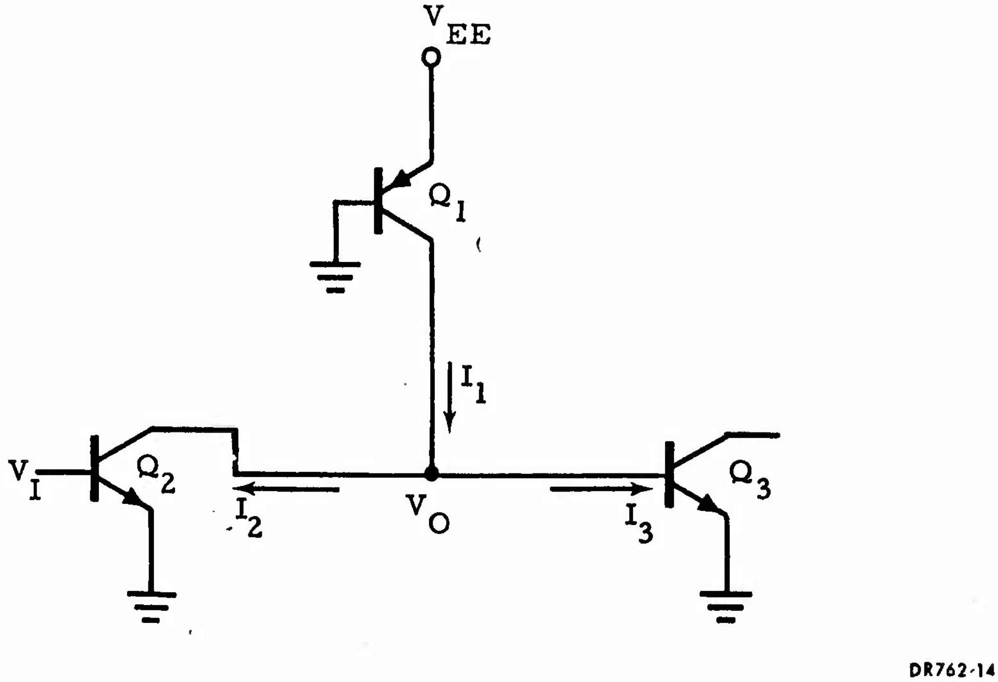

Figure 4-8. Schematic of an I^2L inverter used to define device currents and node voltage.

$$I_2 = I_{CO}\left[\exp(qV_I/kT) - \exp(qV_o/kT)\right] \quad (4\text{-}3)$$

$$I_3 = I_{SCO}\exp(qV_o/2kT) + \left[I_{BhO} + I_{BCO} + I_{BSO}\right]\exp(qV_o/kT) \quad (4\text{-}4)$$

where the saturation currents I_{PO}, I_{CO}, I_{BhO}, I_{BCO}, and I_{BSO} have been previously defined in Section 2.

Substituting Eqs.(4-2) through (4-4) into Eq. (4-1) yields the following

$$I_{PO}\left[\exp(qV_{EE}/kT - \exp(qV_o/kT)\right] = I_{CO}\left[\exp(qV_I/kT) - \exp(qV_o/kT)\right] + I_{SCO}\exp(qV_o/2kT) + \left[I_{BhO} + I_{BCO} + I_{BSO}\right]\exp(qV_o/kT) \quad (4\text{-}4a)$$

Although Eq. (4-4a) describes the I^2L inverter performance adequately, it is unwieldy to use as a circuit design tool. This is partly because I_3 (from Eq.(4-4)) contains the sums of terms that represent hole injection as well as recombination currents. Since hole injection varies with $\exp(qV_I/kT)$ whereas recombination varies as $\exp(qV_I/2kT)$, the calculated value for V_o will depend upon accurate I^2L design modeling if Eq. (4-4a) is to be simplified over some practical range in base supply (i.e., V_{EE}, I_{EE} and V_I).

Fortunately, a significant portion of the Northrop company sponsored I^2L activity during 1975 was directed toward the development of device models. It was found that for the standard wafer process and for the typical range in injection level, the major component of base current is injection of holes from the npn base into the epitaxial layer. This was by no means an obvious result, and it appears to be dependent on the particular wafer process used to fabricate the device.[4]

Using the model for hole injection to account for base current, a design equation similar to that developed by Klaassen[5] can be derived for the general case of nonidentical stages.

4. Horst H. Berger, IEEE Journal of Solid State Electronics, SC-9, 223 (1975).
5. F. M. Klaassen, IEEE Trans. Elec. Devices, ED-22, 145 (1975).

The parameters of interest are the output voltages V_o, as well as the input transition voltages, V_{tr} (i.e., the input voltage which causes the output to change its logic level). The previous expression relating input and output voltages, Eq. (4-4a), can be simplified to the following:

$$I_{po}\left[\exp\left(qV_{EE}/kT\right) - \exp\left(qV_o/kT\right]\approx\right.$$

$$I_{no}\left[\exp\left(qV_I/kT\right) - \exp\left(q\,V_I - V_o\right)/kT + n/\beta\ \exp\left(qV_o/kT\right)\right] \qquad (4\text{-}5)$$

where the npn and pnp saturation currents are indicated by I_{no} and I_{po} and follow the transistor geometry dependence given by:

$$I_{no} \sim S_{C2}^2$$

$$I_{po} \sim L_I$$

where

$$L_I = \text{injector length}$$
$$S_{C2}, S_{C3} = \text{collector areas of } Q_2 Q_3$$
$$n = \left(S_{C3}/S_{C2}\right)^2$$
$$\beta = I_{C3}/I_{B3}$$

From Eq. (4-5), a computer generated transfer curve for any given I^2L inverter can be obtained. The transfer curves of a pair of inverters can also be obtained and plotted on the same axes, which is shown in Figure 4-9 for typical geometries. Note that the noise voltage margin for the pair is indicated graphically. This permits the rapid evaluation of a given design to ensure proper functioning as well as a measure of relative noise margin, using an identical inverter pair as a point of reference.

Figures 4-10 and 4-11 contain transfer curves of typical designs used on the ECOM test chip. Note that noise margin remains relatively constant for a wide range in injection level because the noise margin is primarily controlled by the ratio of I_{no}/I_{po}, which is nearly independent of current and can be adjusted by the ratio of npn collector area to pnp injector length. Because the ratio of these geometries can be well controlled, and in general, will track for a given photoetching process, a worst-case value of noise margin can be specified by design over an LSI chip.

The npn transistor current gain β for a normal range in injection level will similarily be a function of its collector geometry for a given wafer process. This can be shown as follows, where I_C and I_B are the collector and base currents at a given base voltage V_B:

$$I_C = I_{CO}\, e^{qV_B/kT}$$

$$I_B = I_{BO}\, e^{qV_B/kT}$$

Then the npn common-emitter current gain, defined in the active region, is the ratio I_C/I_B as follows:

$$\beta = \frac{I_C}{I_B} = \frac{I_{CO}}{I_{BO}}$$

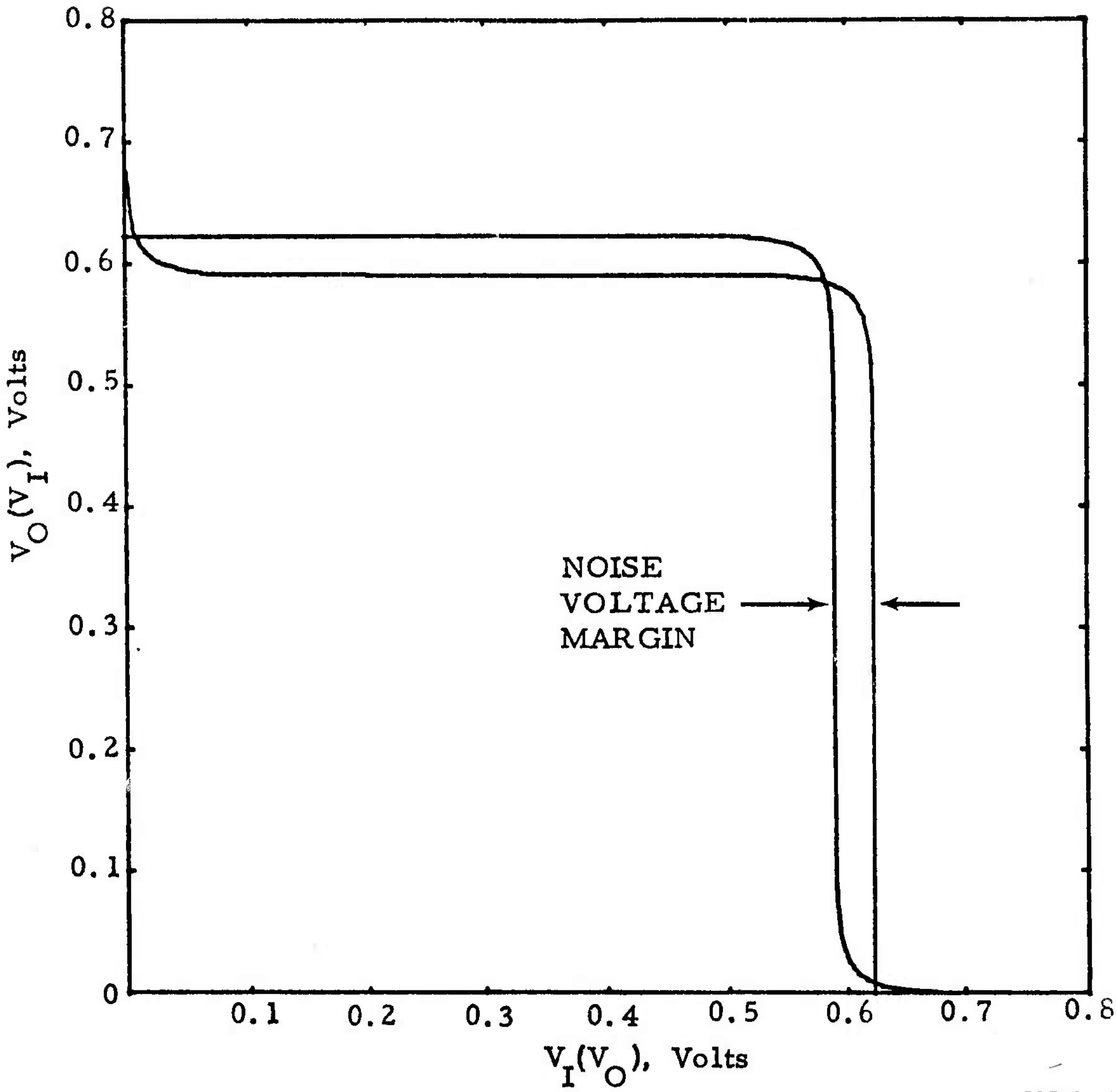

Figure 4-9. DC transfer curves for the driving and driven pair of I^2L inverters.

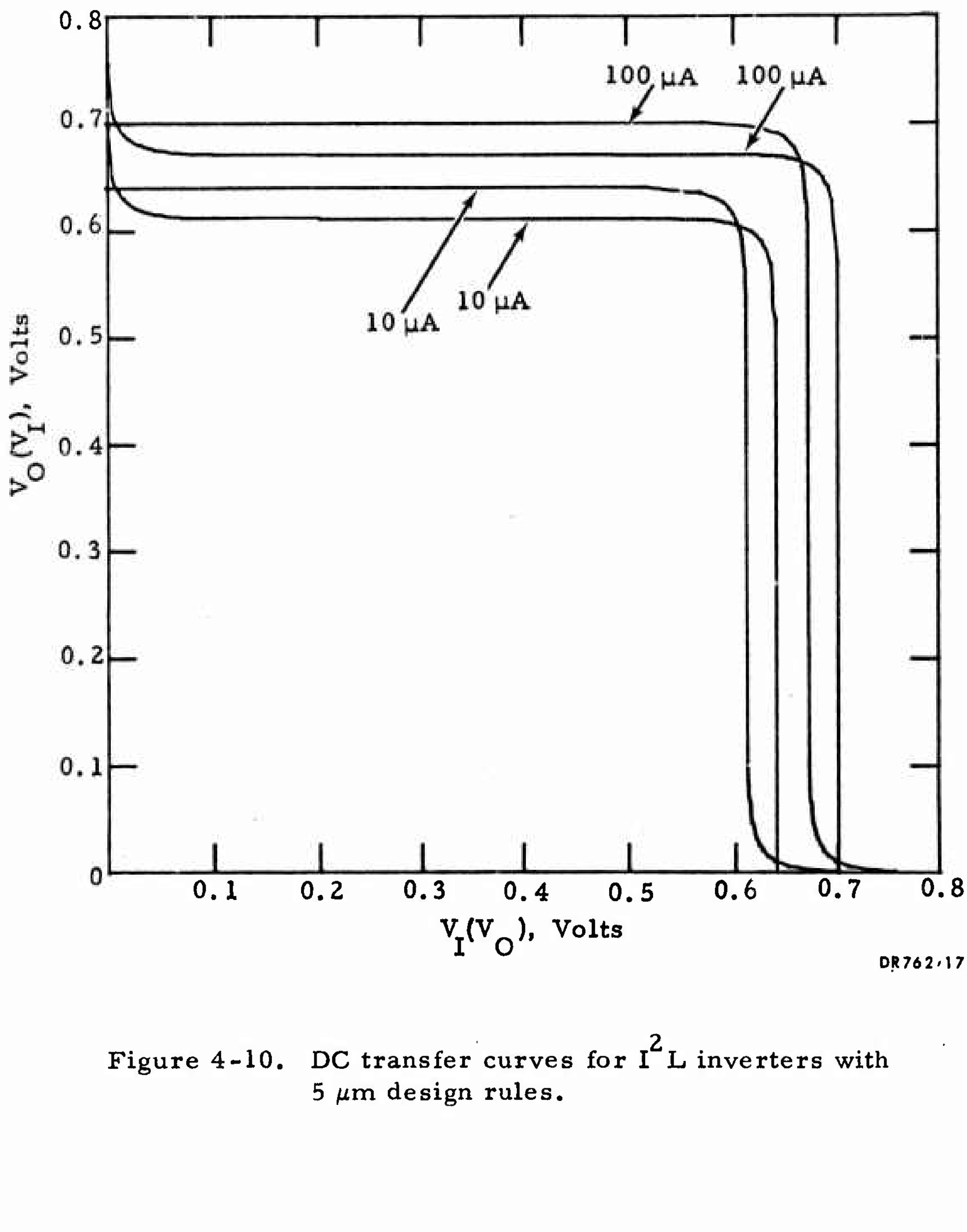

Figure 4-10. DC transfer curves for I^2L inverters with 5 μm design rules.

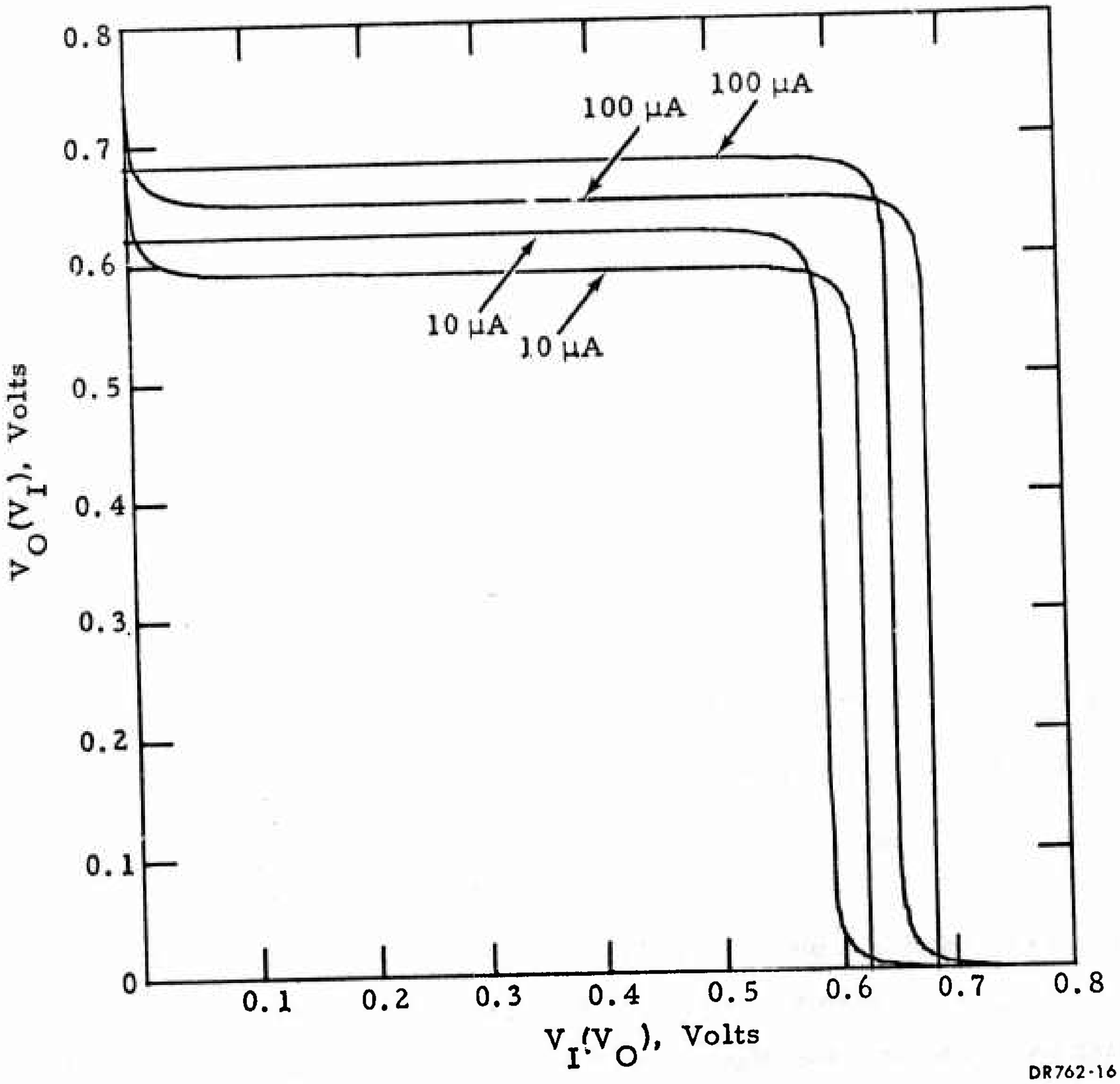

Figure 4-11. DC transfer curves for I^2L inverters with 7.5 μm design rules.

For a given wafer process, it can be shown that:

$$\beta \sim S_C/S_E$$

where S_E, S_C are the npn emitter and collector areas, respectively.

Figure 4-12 contains a layout model used in evaluating the collector-to-emitter area ratio (S_C/S_E) of a multi-collector I^2L gate, as a function of the collector dimension for typical 5µm design rules. This ratio can be expressed as

$$S_C/S_E \approx \frac{\left(\sqrt{S_C} + 2X_C\right)^2}{\left[\sqrt{S_C} + 2X_B + 13\right]\left[N \cdot \sqrt{S_C} + 5 \cdot (N-1) + 2X_B + 23\right]} \qquad (4\text{-}6)$$

where:

$\sqrt{S_C}$	=	side of a square collector (µm)
X_B, X_C	=	junction depths for base or collector (µm)
N	=	fanout

Figure 4-13 contains a plot of Eq. (4-6) versus $\sqrt{S_C}$ with N as the parameter. The ratio S_C/S_E is seen to rise near the origin but saturates at a relatively constant value as the value of $\sqrt{S_C}$ increases. This shows the advantage of minimizing npn emitter area, S_E, by limiting the number of metal cross-overs in the base region.

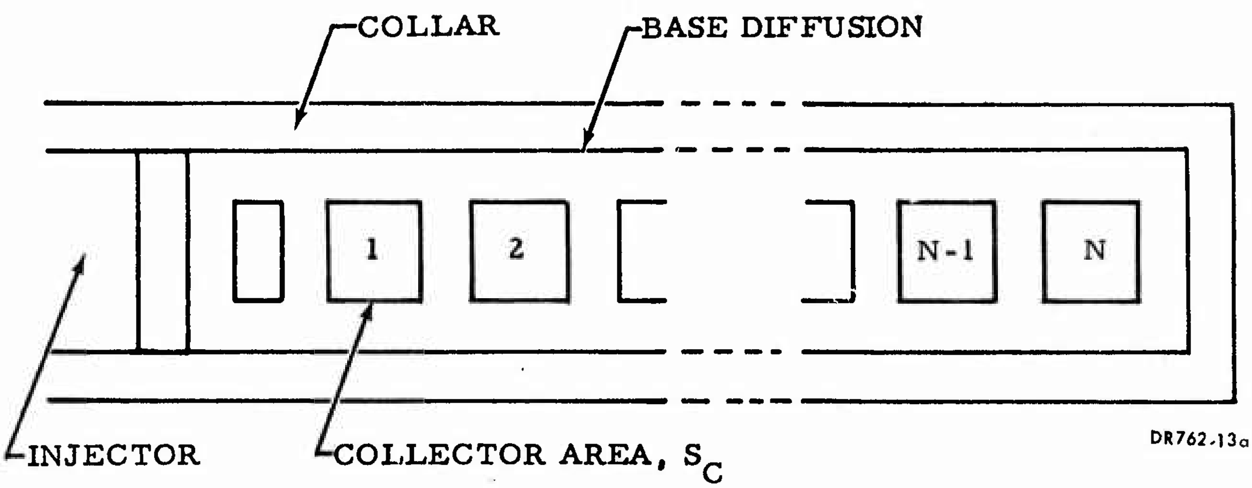

Figure 4-12. Model of multicollector I^2L gate used for evaluation of collector-to-emitter area ratio.

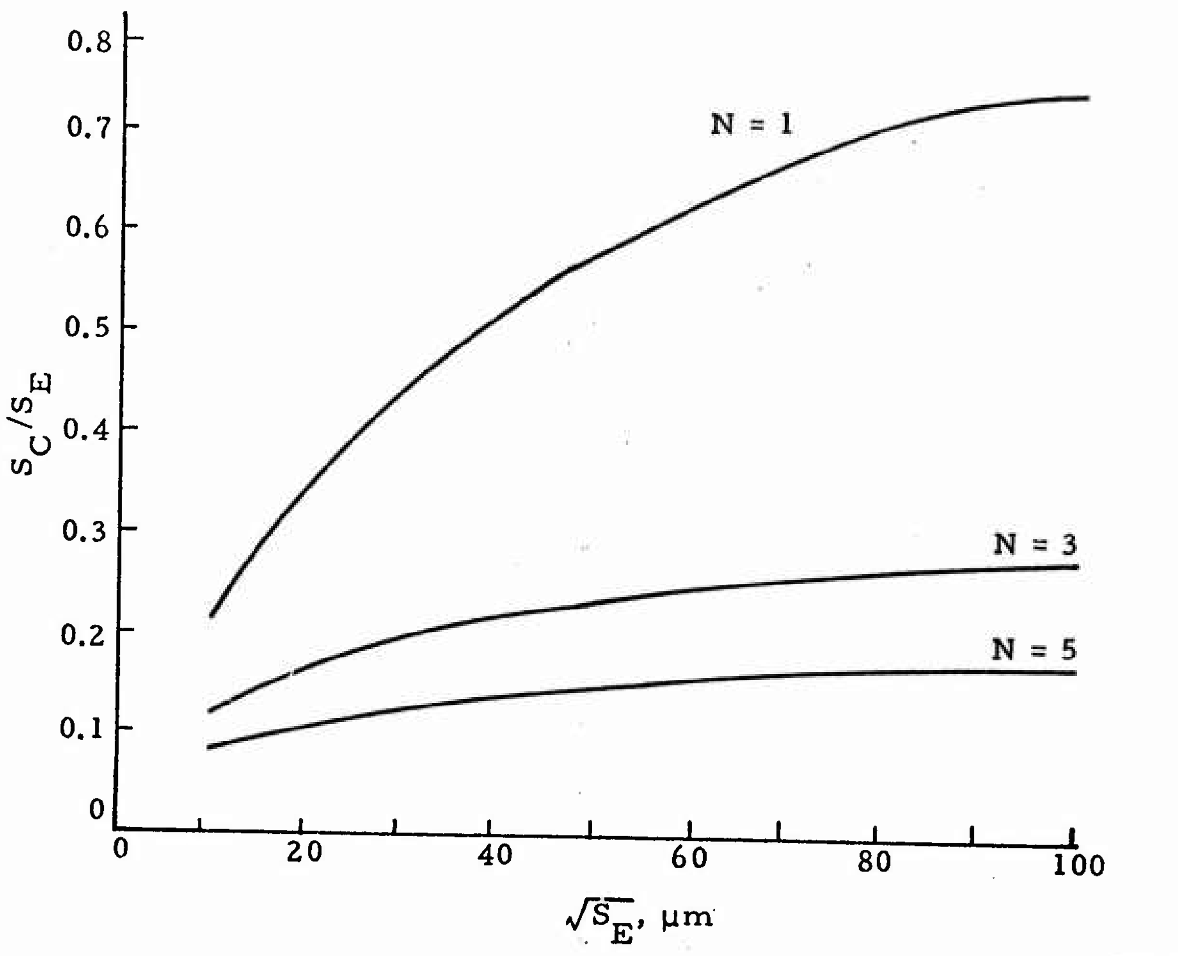

Figure 4-13. Ratio of collector area, S_C, to emitter area, S_E, versus side of square collector, $\sqrt{S_C}$, for the three values of fanout, N.

SECTION 5

EXPERIMENTAL RESULTS

The test chips to be delivered as part of this contract have not yet been fabricated. However, prior to their design, it was necessary to establish typical I^2L design parameters. These parameters were obtained from measurements made on an existing test chip during the normal evaluation of the process from November 1975 through January 1976.

The majority of the data obtained has been used to characterize npn and pnp current gains and to determine typical values of I^2L ring oscillator parameters, such as delay-power product and minimum propagation delay. Measurements were made on an I^2L test inverter to obtain npn and pnp current gains. The important geometries of this inverter are given in Table 5-1. As seen from this table, the test inverter is well representative of a typical I^2L gate using high density LSI layout design rules. All measurements of transistor gain were made in the conventional manner. In other words, for the pnp, the injector was foreward biased with the base and collector grounded. Injector and collector currents were monitored with low impedance ammeters. The ratio of collector current to injector current was calculated as α. For the npn, the base-to-substrate junction was foreward biased and the collector (i. e., most heavily doped n+ region) was reversed biased at approximately 1V. During this measurement, the injector diffusion was left floating such that no significant minority carrier density gradient was established between it and the npn base region, eliminating that component of diffusion current. Ammeters were used to sample collector and base currents, and the ratio taken to be β.

Figure 5-1 contains a plot of typical npn I-V data. The base and collector currents are plotted versus the base-emitter voltage. The figure includes experimental data for various devices, as indicated, as well as computer calculations. Good agreement was obtained between the I-V data and the

TABLE 5-1. TEST INVERTER GEOMETRIES

pnp Injector Basewidth	W_{BO}	3 μm
pnp Injector Diffusion Area	S_I	180 μm
pnp Injector Contact Area	A_{CP}	$52\ \mu m^2$
npn Emitter Area	S_E	$450\ \mu m^2$
npn Collector Area	S_C	$100\ \mu m^2$
npn Collector-to-Emitter Area Ratio	S_C/S_E	0.22
npn Base Contact Area	A_C	52 μm

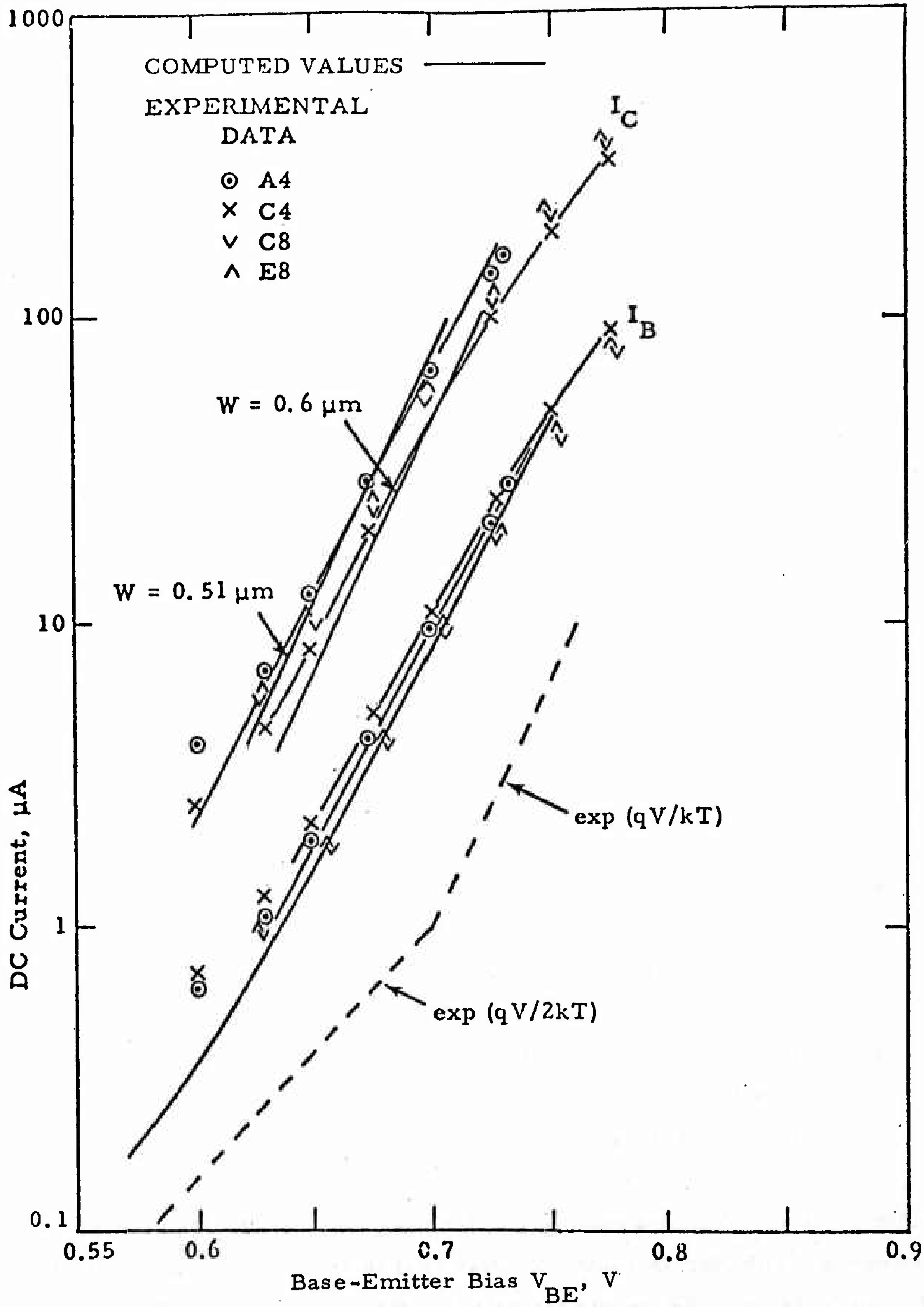

Figure 5-1. Comparison of computed and experimental current-voltage characteristics for an I^2L npn transistor.

computer calculations made with the process parameters that correspond to the wafer lot under evaluation.

Table 5-2 contains a brief summary of the data obtained for npn and pnp current gains. Measurements for both an epitaxial and a nonepitaxial process are given; however, it should be noted that these data are preliminary and should not be interpreted as typical of the NRTC process. Instead, they are more likely to be representative of the relative difference between the epitaxial process and the preliminary nonepitaxial process which has not been fully established.

The results of these transistor measurements indicate the following tentative conclusions can be made:

- the pnp current gain for the nonepitaxial process is approximately 2/3 the value for the epitaxial process, due primarily to the higher base current resulting from hole injection into the nonepitaxial substrate.

- the npn current gain for the nonepitaxial process is approximately 1/2 of the value for the epitaxial process, due to increased base current as discussed above.

- the npn collector breakdown voltages are approximately equal for both processes, as expected from the similarity in base diffusion profiles.

Table 5-2 also contains a summary of the ring osciallation data for both processes. The ring oscillator consists of inverters with a single collector of 10μm x 38μm. The results indicate that the delay power product and minimum delay are approximately 0.35 pJ and 15 ns respectively, which are

TABLE 5-2. I^2L TEST DATA FOR EPITAXIAL AND NONEPITAXIAL WAFERS, REPRESENTING LOT 10-5-29

I^2L Wafer Process	Transistor Data			Ring Oscillator Data	
	pnp	npn		Delay x Power	Minimum Delay
	α	β	BV_{CEO}		
Epitaxial	0.65	7.5	5 V	0.35 pJ	15 ns
Non epitaxial	0.45	3	6 V	0.50 pJ	25 ns

typical values. However, the results of the nonepitaxial process show that the delay-power of 0.50 pJ almost equal to the standard epitaxial process. In addition, the minimum delay of 25 ns is less than a factor of 2 greater than that for the epitaxial process. In fact, this value of minimum delay is comparable to those values reported for the early epitaxial work, before diffusion profiles and epitaxial film parameters had been optimized. It is not unlikely that some improvement can similarly be made for the nonepitaxial process.

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